Exp. No:
Date :

LIGHT-DEPENDENT RESISTOR (LDR) CHARACTERISTICS AND OBJECT COUNTER USING LDR AS SENSOR

Aim :

(a) To determine the characteristics of LDR.

(b) Construction of object counter using LDR as sensor.

Part I.

Light-Dependent Resistor (LDR) Characteristics

Theory:

A **photoresistor or LDR** is an electronic component whose resistance decreases with increasing incident light intensity. It can also be referred to as a **light-dependent resistor** (LDR), **photoconductor**, or **photocell**. A photoresistor is made of a high-resistance semiconductor. If light falling on the device is of high enough frequency, photons absorbed by the semiconductor give bound electrons enough energy to jump into the conduction band. The resulting free electron (and its hole partner) conduct electricity, thereby lowering resistance.

Cadmium sulfide (CdS) cells rely on the material's ability to vary its resistance according to the amount of light striking the cell. The more light that strikes the cell, the lower the resistance. Although not accurate, even a simple CdS cell can have a wide range of resistance from less than 100 Ω in bright light to in excess of 10 MΩ in darkness. Many commercially available CdS cells have a peak sensitivity in the region of 500nm - 600nm (green light). The cells are also capable of reacting to a broad range of frequencies, including infrared (IR), visible light, and ultraviolet (UV). They are often found on street lights as automatic on/off switches.

Apparatus Required:

(i) Multi- meter (to be used as Ohm meter)

(ii) Measurement scale

(iii) LDR

(iv) 60 Watts bulb.

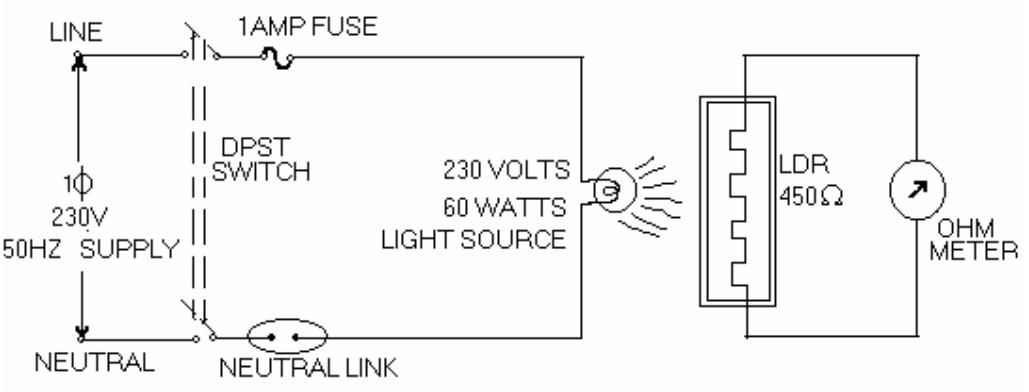

Fig.1. Characteristics of LDR

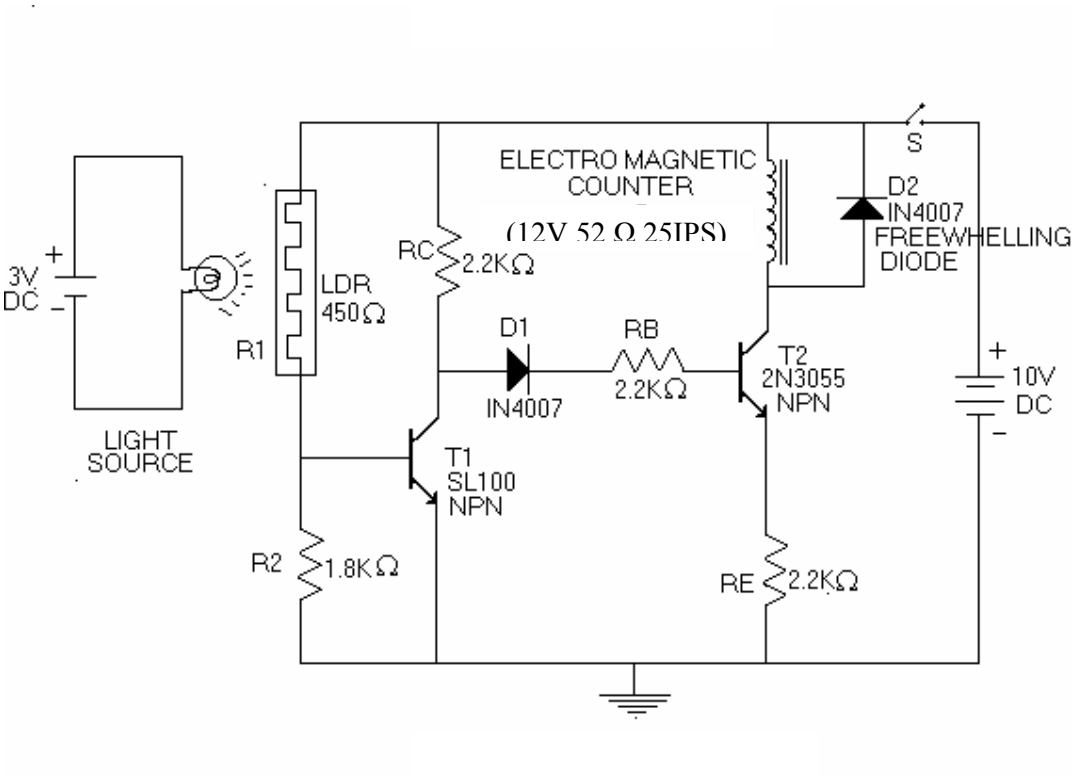

Fig.2 Object Counter Circuit using LDR as sensor

Procedure:

1. Set up a 60W lamp on the bench to act as a light source as shown in Fig.1.
2. Connect the multi-meter to the LDR and adjust it to a suitable resistance range.
3. Measure the dark resistance of the LDR after covering the LDR by a black piece of cloth.
4. Now place the LDR at different distances (r) from the lamp and measure its resistance.
5. You should end up with a table showing distance and resistance.

Plot a graph to show how the resistance (*y*-axis) varies with distance (*x*-axis) as shown in model graph (Fig.3). The light intensity (E) is believed to be inversely proportional to the square of the distance (r) from the light source ($E = \frac{1}{r^2}$). Therefore, complete the table with calculated $\frac{1}{r^2}$ values. Plot a graph to show how the resistance varies with light intensity by plotting resistance against $\frac{1}{r^2}$ as shown in model graph (Fig.4).

Part II

Object Counter Using LDR

Apparatus required

(i) 0 – 30 volts dual D.C power supply

(ii) 3 volts dc motor (FHP)

(iii) Electromagnetic counter (12 volts , 52 ohms , 25 IPS)

(iv) 2N3055 NPN power transistor

(v) SL100 NPN transistor

(vi) 1N4007 Junction diode ------- 2 Nos.

(vii) Resistors: 1.8 kΩ,1/2 watt; 2.2 kΩ ,1/2 watt.

Theory:

The circuit diagram shown in Fig.2 is an object counter that uses LDR as light sensor. Under normal condition when the object is not present, the LDR is exposed to the light source and hence the LDR resistance is low. Therefore, the voltages drop across the

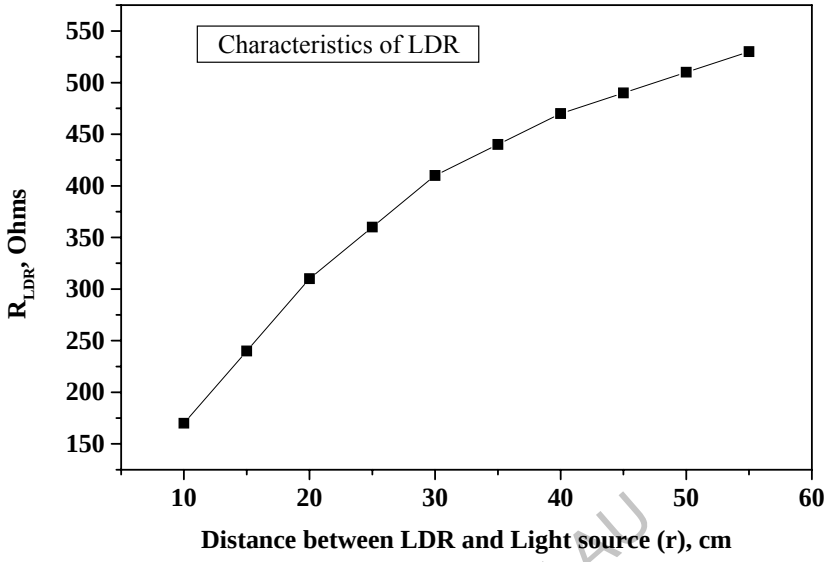

Fig.3. LDR Resistance (R_{LDR}) versus Distance (r)

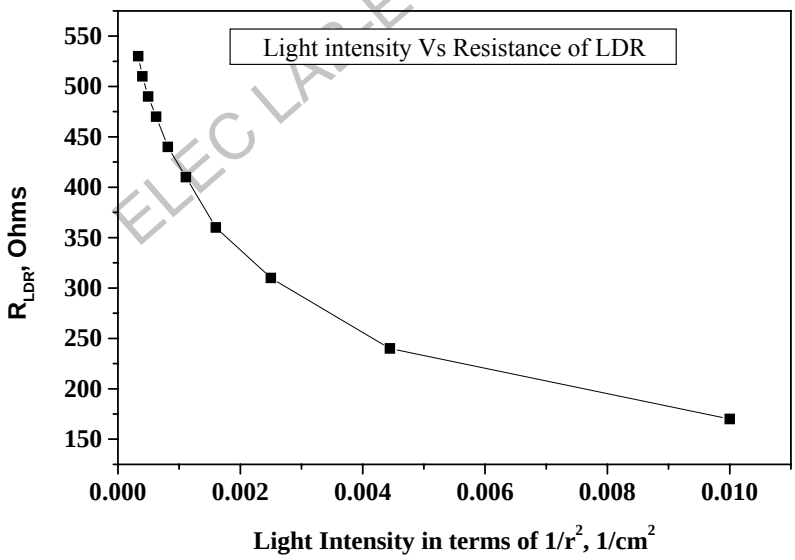

Fig.4. LDR Resistance (R_{LDR}) versus Light Intensity

(Light intensity is represented in terms of $\frac{1}{r^2}$)

1.8 kΩ (Base to emitter Voltage V_{BE1} of Transistor T1) is more than 0.7V. This voltage can be calculated by potential divider rule and is as follows:

$$V_{BE1} = \frac{R2}{R2 + R_{LDR}} V_{CC} \qquad (V_{CC} = 10V \text{ here})$$

This voltage is sufficient enough to drive the transistor T1 into saturation. This results in a low collector voltage V_{C1} (around 0.2V) which is not sufficient to switch on the Transistor T2. However, when the light is interrupted by a moving object, the LDR resistance increases momentarily thus reducing V_{BE1} below 0.7V. This makes the transistor T1 off thus raising the the collector voltage V_{C1} to 10V approximately. This switches on the transistor T2 thus energizing the counter coil to increment the count. These actions are summarized in the following table.

Object Presence	**LDR exposed to light**	**LDR Resistance**	V_{BE1}	**Status of transistor T1**	V_{C1}	**Status of transistor T2**	**Counter status**
No	Yes	Low	>0.7V	On	0.2V	Off	No increment
Yes	No	High	<0.7V	Off	10V	On	Incremented

A conveyor belt (elastic belt) is used to achieve fast movement of an object in this experiment. The speed of the movement of the object is controlled by the speed of the dc motor. A 3 volts dc supply is applied to the dc motor and the light source. Energise the sensor circuit with 10 volts dc supply. When the motor is switched on, the conveyor belt moves and hence object moves. The light source and the LDR are placed diametrically opposite to each other in opposite sides of the conveyor belt and when the object crosses this arrangement, the light falling on the LDR is momentarily interrupted.

Table 1. LDR Characteristics

Distance between LDR and source r (cm)	$\frac{1}{r^2}$	R_{LDR} (Ohms)
5		
10		
15		
20		
25		
30		
35		
40		
45		
50		

Table 2. Object Counter Circuit experimental verification data

Object Presence	**LDR exposed to light**	**LDR Resistance**	V_{BE1}	**Status of transistor T1**	V_{C1}	**Status of transistor T2**	**Counter status**
No							
Yes							

Procedure:

(1) Connect the circuit as shown in Fig.2

(2) Energise the circuit with 10V D.C power supply. Switch on the light source. However, do not switch on the supply to the conveyor.

(3) Manually adjust the conveyor so that the object does not interrupt the light source from falling on the LDR. Measure the voltages V_{BE1} and V_{C1} and tabulate the values in the table. Indicate the status of the transistor switches and counter in the table.

(4) Manually adjust the conveyor so that the object does interrupt the light source from falling on the LDR. Measure the voltages V_{BE1} and V_{C1} and tabulate the values in the table. Indicate the status of the transistor switches and counter in the table.

(5) Now, switch on the supply to the conveyor and note down the count after 10 revolutions. Justify your result.

Result:

The characteristics of LDR were determined. The resistance of the LDR decreases with increasing light intensity. The dark resistance of the given LDR was measured to be ------Ohms. An object counter was constructed using LDR sensor and transistor switches. The object counting is tested and found to be working satisfactorily.

Exercises :

1. What are the materials used for fabricating LDR?
2. What is the relationship between resistance of the LDR and the light intensity?
3. What will happen if LDR and resistor R2 are interchanged?
4. What are the applications of LDR?

APPENDIX
SPECIFICATIONS OF ELECTRONIC DEVICES

SL100 NPN TRANSISTOR

BVCBO	60 volts.
BVCER	50 volts.
BVEBO	60 volts.
I_c	0.5 amps.
Max. Collector dessipation	4 watts.
I_{surge}	1 amp
I_{CBO}	1 μA

h_{fe} 40/300 at V_{CE} = 5 Volts , I_C = 150 mA.

2N3055 NPN TRANSISTOR

VCBO	100 volts
VCER	70 volts
VCEO	60 volts
VCEV	90 volts
VEBO	07 volts
I_C	15 amp
I_B	07 amp
Dissipation	115 watts
Operating temp. range	- 65°C to + 200°C

1N 4007 DIODE

VRM(rep)	1000 volts
VRM(working)	1000 volts
VR	1000 volts
VRM(non - rep)	1500 volts
V_r	700 volts
I_o	1 amp
I_{FM}	30 amp

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MEASUREMENT OF INPUT IMPEDANCE, OUTPUT IMPEDANCE, VOLTAGE GAIN OF GIVEN RC COUPLED COMMON EMITTER AMPLIFIER

Aim

To determine the current gain, voltage gain, input impedance, output impedance and bandwidth of a RC coupled common emitter amplifier circuit.

Theory

The common emitter circuit has good voltage gain with phase inversion i.e. the output voltage decreases when the input voltage increases and vice-versa. The CE circuit also has good current gain and power gain and relatively high input and low output impedance. As a voltage amplifier the CE circuit is by far the most frequently used of all 3 basic transistor configurations.

In the amplifier circuit shown in **Fig.1,** R_E is the thermal stabilizing resistance, C_E is the bypass capacitor. The collector circuit resistance R_C is kept at 1 kΩ and R_1 and R_2 form the potential divider. The load R_L is coupled by a capacitor to block any d.c voltage at the load. Similarly, the a.c. input signal is input to the amplifier through a coupling capacitor C_C.

Procedure

<u>To obtain the input impedance</u> Z_{in}

1. The connections are made as per the circuit diagram shown in **Fig.2.**
2. Set the function generator input voltage as 20mV and frequency as 1kHz.
3. Note down the output voltage of the amplifier keeping $\mathbf{R_X}$ =0.
4. Now, increase $\mathbf{R_X}$, till the output voltage is reduced to half. Note down the reading $\mathbf{R_X}$.

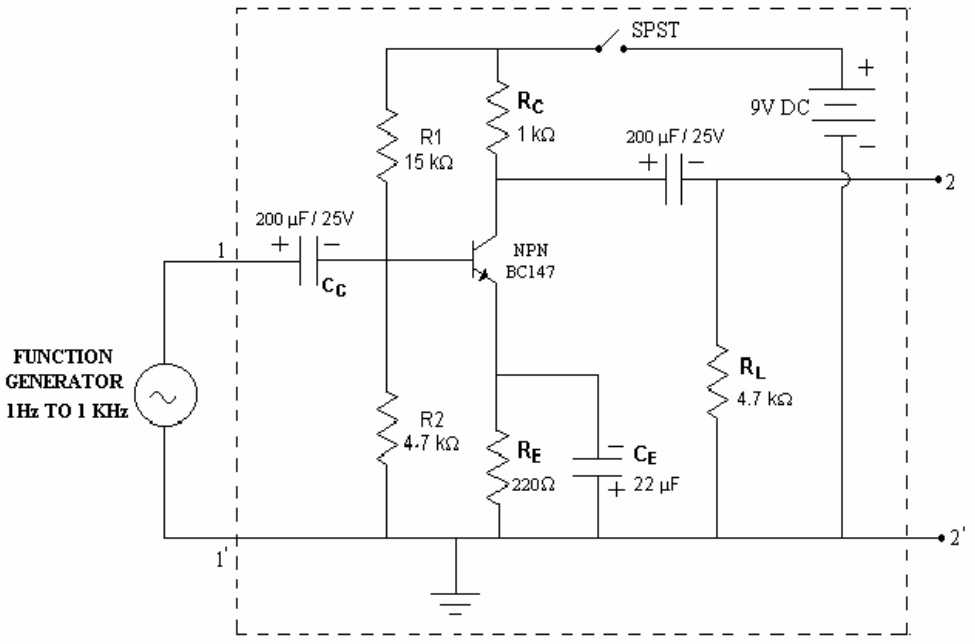

Fig.1. Circuit Diagram of RC coupled Common Emitter Amplifier

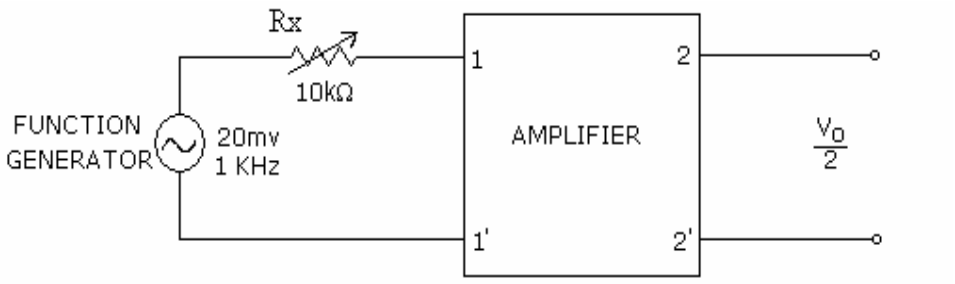

FIGURE 2. TO MEASURE THE INTERNAL RESISTANCE OF THE AMPLIFIER

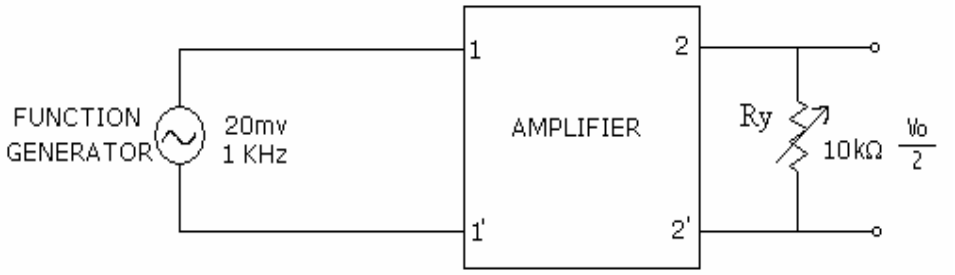

FIGURE 3. TO MEASURE THE OUTPUT RESISTANCE OF THE AMPLIFIER

This $\mathbf{R_X}$ value gives the input impedance (Z_{in})of the amplifier circuit. This is due to the fact when the value of $\mathbf{R_X}$ equals the input impedance Z_{in} of the amplifier only half the input voltage appears across Z_{in} and therefore the output voltage reduces to half ($\mathbf{V_o/2}$) since the voltage gain ($\mathbf{A_v}$) is constant and the frequency is maintained constant at 1kHz.

Input Voltage V_{in}	$\mathbf{R_X}$	Measured Output Voltage
20mV	0	(Say $\mathbf{V_o}$)
20mV		**($\mathbf{V_o/2}$)**

Measured input impedance at 1kHz (Z_{in} **) = ……..**

<u>To obtain the output impedance</u> *Zo*

1. The connections are made as per the circuit diagram shown in **Fig. 3**.
2. Set the function generator input voltage as 20mV and frequency as 1kHz.
3. Set R_y = 10 kΩ so that *Zo* << R_y and note down the output voltage $\mathbf{V_o}$.
4. Now, decrease $\mathbf{R_Y}$, till $\mathbf{V_o}$ becomes $\mathbf{V_o/2}$. At this point, the load voltage becomes half since the present value of $\mathbf{R_Y}$ equals *Zo* of the amplifier.
5. The experimental setup shown in **Fig.3** is used to determine the output impedance of the amplifier circuit. Considering the Thevenin's equivalent circuit to the output side, we find that when the value of the resistance in the decade box, $\mathbf{R_Y}$ equals *Zo* of the amplifier, the voltage is divided equally and hence $\mathbf{V_o}$ becomes $\mathbf{V_o/2}$.

Input Voltage V_{in}	$\mathbf{R_Y}$	Measured Output Voltage
20mV	10 kΩ	(Say $\mathbf{V_o}$)
20mV		**($\mathbf{V_o/2}$)**

Measured output impedance at 1kHz (*Zo* **) = ……..**

Table 1 Frequency response characteristics

$V_{in} = 20mV$

S.No	Frequency (Hz)	Output Voltage V_o (Volts)	Voltage Gain Vo / Vin	Gain in dB 20 log (Vo/Vin)
1	20			
2	40			
3	60			
4	80			
5	100			
6	200			
7	400			
8	600			
9	800			
10	1000			
11	2000			
12	4000			
13	6000			
14	8000			
15	10000			
16	20000			
17	40000			
18	60000			
19	80000			
20	100k			
21	200k			

To Determine Bandwidth

1. The connections are made as per the circuit diagram shown in **Fig. 1**.
2. The signal generator input voltage is maintained at 20 mV constant and its frequency is varied from 10Hz to 100kHz.
3. Corresponding output voltages are noted down at each frequency.
4. Frequency response curve is plotted on a semilog sheet taking **log f** along X-axis and the **Voltage gain in dB= 20 log V_o/V_{in}** along Y-axis.

To Determine current gain A_I

We know that the voltage gain A_V is given as $A_V = \frac{A_I \times Z_o}{Z_{in}}$. Therefore, the current gain $A_I = \frac{A_V \times Z_{in}}{Z_o}$. At the frequency of 1kHz, we have already obtained the voltage gain A_V, input impedance Z_{in} and output impedance Z_o. Using the values, the current gain can be calculated.

Result

The voltage gain A_V, input impedance Z_{in}, output impedance Z_o and bandwidth of the common emitter amplifier were calculated. The current gain A_I was estimated from the measured values of voltage gain, input impedance, and output impedance. The measured amplifier parameters are summarized below.

Amplifier parameter	Measured Values	Unit
Input impedance at 1kHz (Z_{in})		
Output impedance at 1kHz (Z_o)		
Bandwidth		
Voltage gain at 1kHz (A_V)		
Current gain at 1kHz (A_I)		

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DETERMINATION OF h-PARAMETERS OF THE GIVEN TRANSISTOR AND ANALYSIS OF AN AMPLIFIER CIRCUIT USING HYBRID EQUIVALENT CIRCUIT

Aim:

1. To experimentally obtain the hybrid a.c equivalent circuit of the given transistor by calculating the h-parameters from the input and output characteristics of the transistor.

2. To analyze the given RC coupled amplifier employing the given transistor using the hybrid a.c equivalent circuit of the transistor and determine analytically the voltage gain of the given amplifier.

3. To conduct suitable experiments on the given amplifier and measure the voltage gain of the amplifier and compare the measured voltage gain with the analytical gain calculated.

Apparatus Required:

1. Signal generator
2. DC power supply [0-30V D.C]
3. A.C Voltmeter [0-10V]
4. Transistor –SL100
5. Resistors and capacitors to construct the circuit shown in Fig.9.

Theory:

Two Port Network: To determine the hybrid equivalent circuit, consider a two-port network as shown in Fig.1. We may select any two of the quantities as independent variable and express the remaining two dependent variables in terms of independent variables. Fig.2 shows the equivalent circuit of any two port network. In this network,

$$v_1 = h_{11} i_1 + h_{12} v_2$$

$$i_2 = h_{21} i_1 + h_{22} v_2$$

where h_{11}, h_{12}, h_{21} and h_{22} are called hybrid parameters or simply h-parameters.

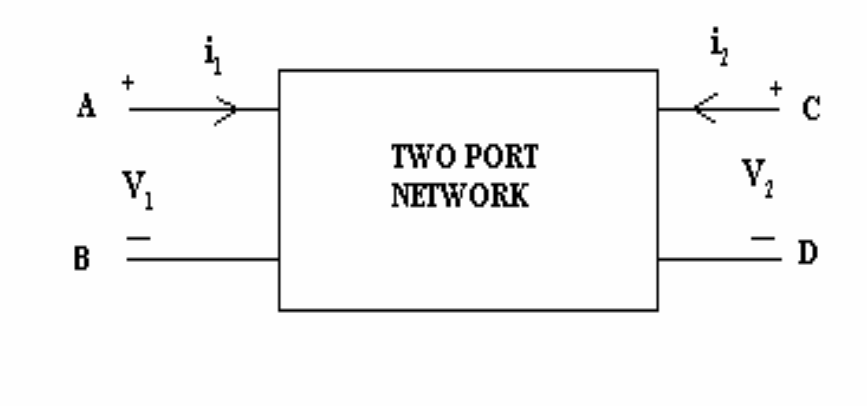


Fig.1 Two port network

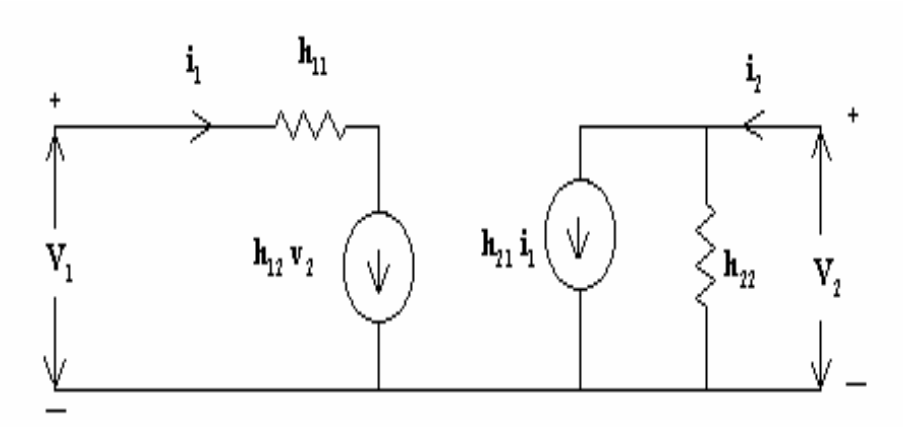


Fig 2. Hybrid equivalent circuit of two port network

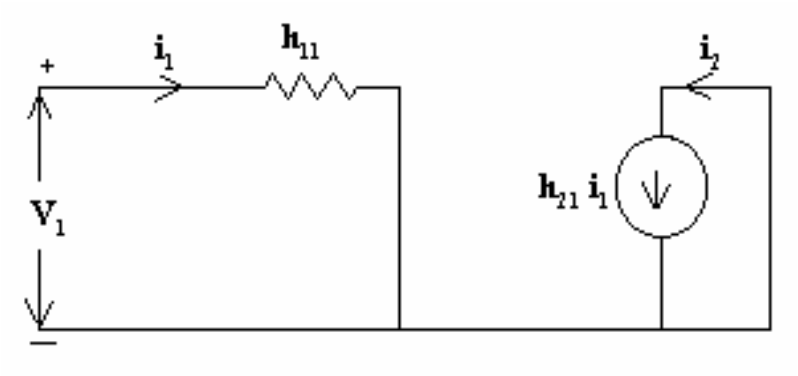


Fig.3 Hybrid equivalent circuit of two port network with output shorted

$h_{11} = \frac{v_1}{i_1}$ with $v_2 = 0$

This gives the a.c input resistance with output shorted for a.c. (Fig.3)

$h_{12} = \frac{v_1}{v_2}$ with $i_1 = 0$

This gives the reverse voltage transfer ratio with the input open for a.c (Fig.4)

$h_{21} = \frac{i_2}{i_1}$ with $v_2 = 0$

This gives the forward current gain with output shorted for a.c (Fig.3)

$h_{22} = \frac{i_2}{v_2}$ with $i_1 = 0$

This gives the output conductance with the input open for a.c (Fig.4)

CE Transistor as two port network: Consider a simple common emitter transistor configuration shown in Fig.5. Select the base current (I_B) and Collector to Emitter voltage (V_{CE}) as independent variables. The input voltage (V_{BE}) and output current (I_C) are considered to be dependent on the above said independent parameters. This circuit can be well considered to be a two port network for it has the emitter common to both input and output and linear for small signals. Fig.6 shows the equivalent circuit of common emitter configured transistor.

$V_{BE} = f(I_B, V_{CE})$

$I_C = f(I_B, V_{CE})$

Now, the equations of the circuit (Fig.6) can be written as,

$v_{be} = h_{ie} i_b + h_{re} v_{ce}$

$i_c = h_{fe} i_b + h_{oe} vce$

Now, if one wishes to obtain the a.c equivalent circuit of the given transistor it becomes necessary to measure the h-parameters h_{ie}, h_{re}, h_{fe} and h_{oe}. From the above said equations, we can write,

$h_{ie} = \frac{v_{be}}{i_b}$ with $v_{ce} = 0$. The output should be shorted for a.c to make $v_{ce} = 0$. Physically, it means that output voltage should not be allowed to change. This can be

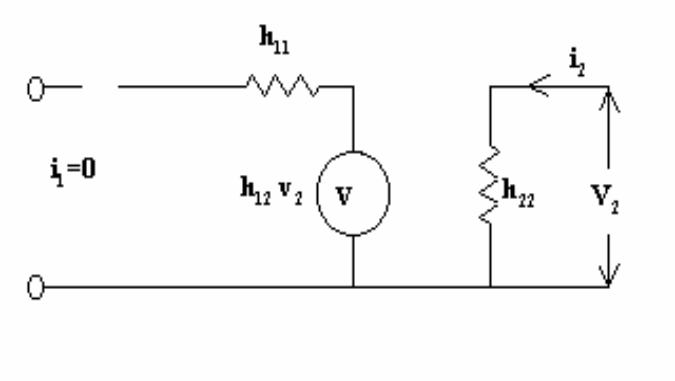


Fig.4 Hybrid equivalent circuit of two port network with input open circuited

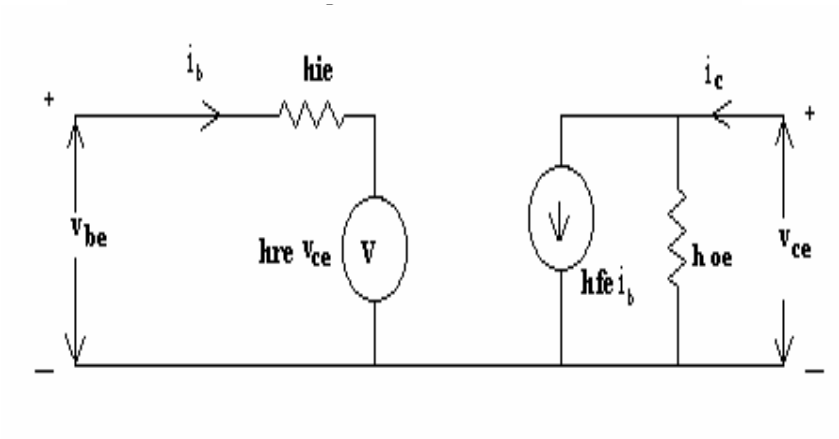


Fig.5 CE Configured Transistor circuit

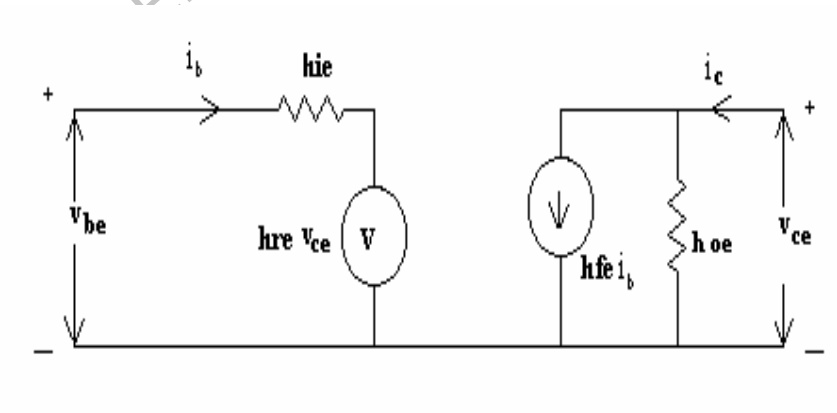


Fig.6 Hybrid equivalent circuit of CE configured transistor

achieved by maintaining V_{CE} constant. However, input voltage should be given a small change (v_{be} or ΔV_{BE}) and the change in input current (i_b or ΔI_B) should be observed to calculate h_{ie} the a.c input resistance of the transistor. It is obvious from the above discussion that h_{ie} can be calculated from the input characteristics of the given transistor where in I_B versus V_{BE} is plotted keeping V_{CE} constant. So, the input a.c resistance of the transistor is $h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}$ with V_{CE} constant.

$h_{re} = \frac{v_{be}}{v_{ce}}$ with $i_b = 0$. The input should be opened for a.c. to make $i_b = 0$. Physically, it means that input current should not be allowed to change. This can be achieved by maintaining I_B constant. However, input voltage should be given a small change (v_{be} or ΔV_{BE}) and the change in output voltage (v_{ce} or ΔV_{CE}) should be observed to estimate h_{re}. It is obvious from the above discussion that h_{re} can be calculated from the input characteristics of the given transistor where in I_B versus V_{BE} is plotted for a set of constant V_{CE} values.

$h_{fe} = \frac{i_c}{i_b}$ with $v_{ce} = 0$. The output should be shorted for a.c to make $v_{ce} = 0$. Physically, it means that output voltage should not be allowed to change. This can be achieved by maintaining V_{CE} constant. However, input current should be given a small change (i_b or ΔI_B) and the change in output current (i_c or ΔI_C) should be observed to calculate h_{fe}, the forward a.c current gain of the transistor. It is obvious from the above discussion that h_{fe} can be calculated from the output characteristics of the given transistor where in I_C versus V_{CE} is plotted for a set of constant I_B values.

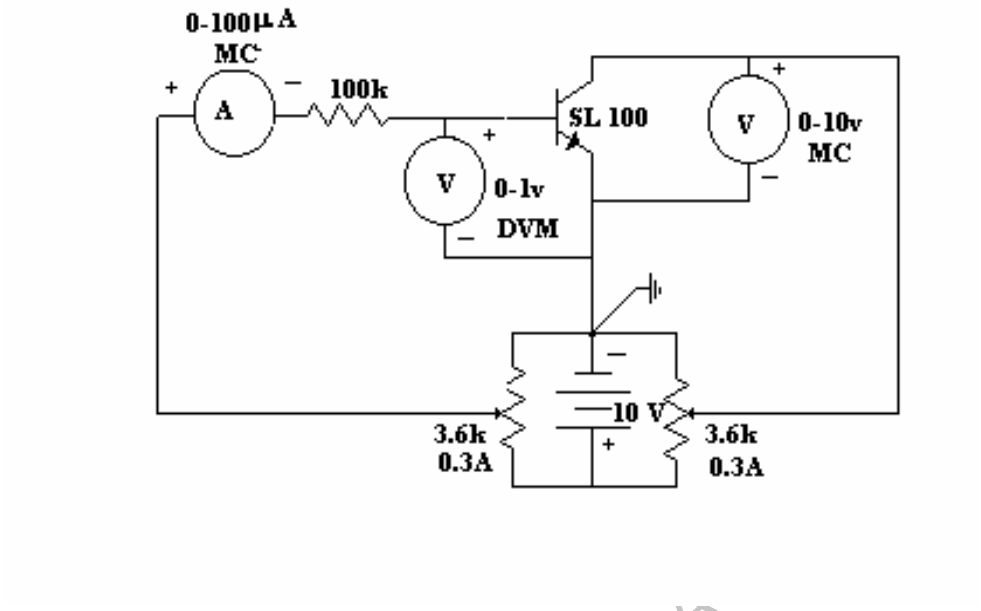


Fig.7 Experimental Circuit diagram for Input characteristics of CE transistor

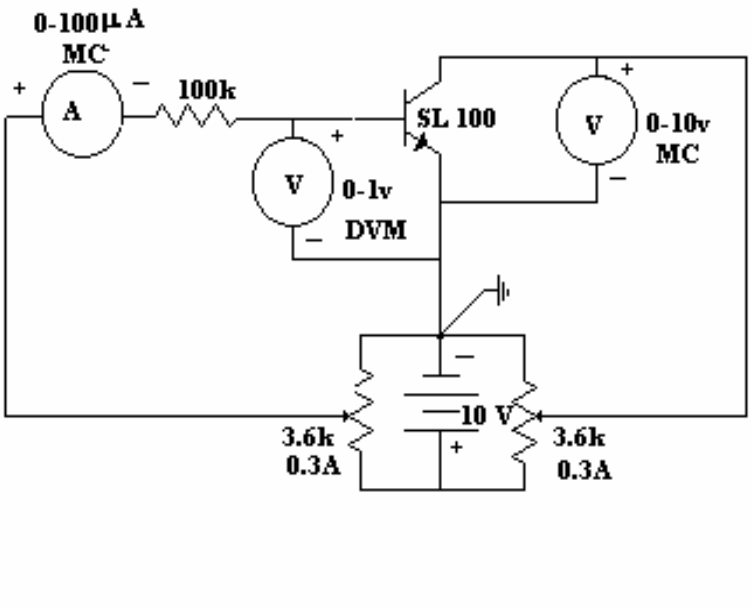


Fig. 8. Experimental circuit diagram for Output characteristics of CE transistor

$h_{oe} = \dfrac{i_c}{v_{ce}}$ with $i_b = 0$. The input should be opened for a.c. to make $i_b = 0$. Physically, it means that input current should not be allowed to change. This can be achieved by maintaining I_B constant. However, output current should be given a small change (i_c or ΔI_C) and the change in output voltage (v_{ce} or ΔV_{CE}) should be observed to estimate h_{oe}. It is obvious from the above discussion that h_{oe} can be calculated from the output characteristics of the given transistor where in I_C versus V_{CE} is plotted for a constant I_B value.

Procedure:

Determination of h_{ie} :

1. The measured data of the input characteristics from the circuit (Fig.7) are given in Table1.
2. Draw the I_B versus V_{BE} characteristics as shown in the model graph given as Fig.M1.

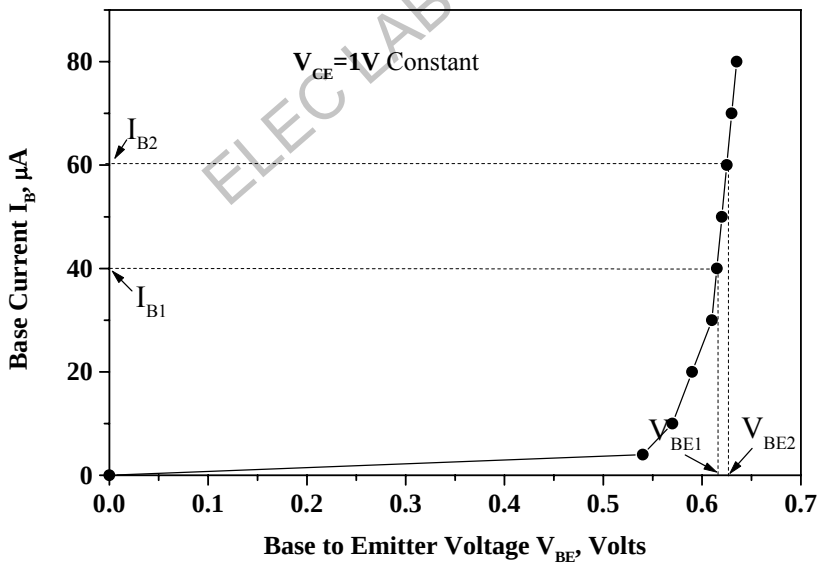


Fig.M1. I_B versus V_{BE} characteristics of given BJT

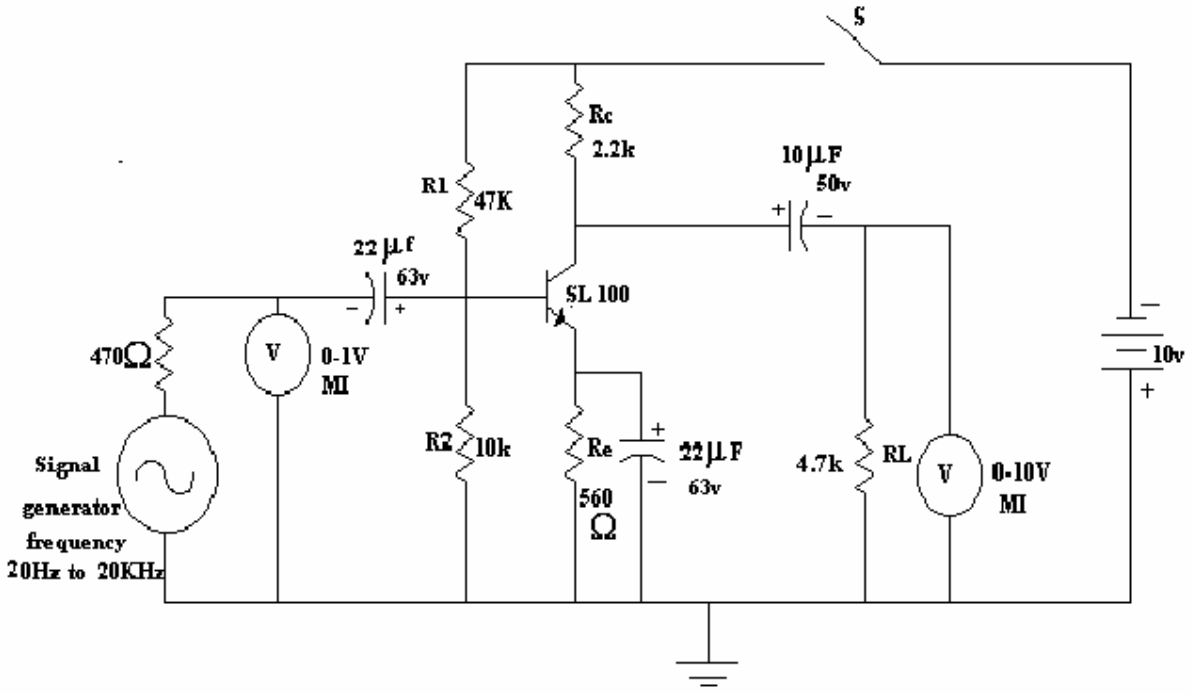


Fig.9 Experimental circuit diagram of RC coupled Common Emitter Amplifier

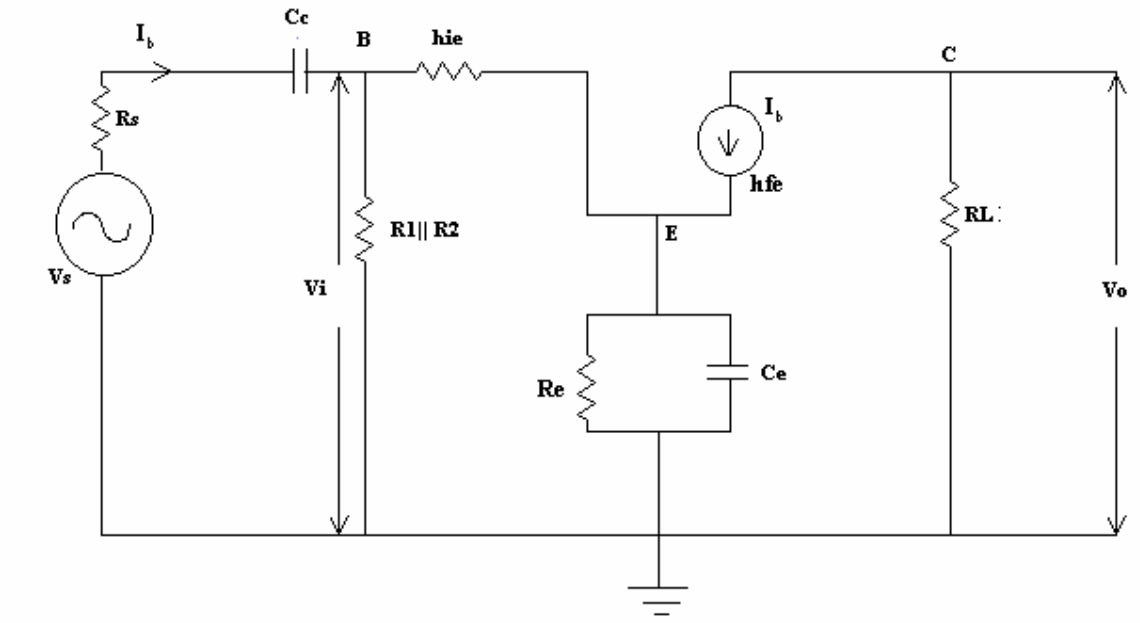


Fig.10 Hybrid equivalent circuit of RC coupled Common Emitter Amplifier

3. Mark the points I_{B1}, I_{B2}, V_{BE1} and V_{BE2} as shown in the Fig.M1 and note down the values.
4. $\Delta V_{BE} = V_{BE2} - V_{BE1}$ and $\Delta I_B = I_{B2} - I_{B1}$.
5. Calculate the a.c input resistance of the given transistor using the formula $h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}$.

Determination of h_{re}:

1. The measured data of the input characteristics are given in Table1.
2. Draw the I_B versus V_{BE} characteristics as shown in the model graph given as Fig.M2 for two different values of V_{CE}.

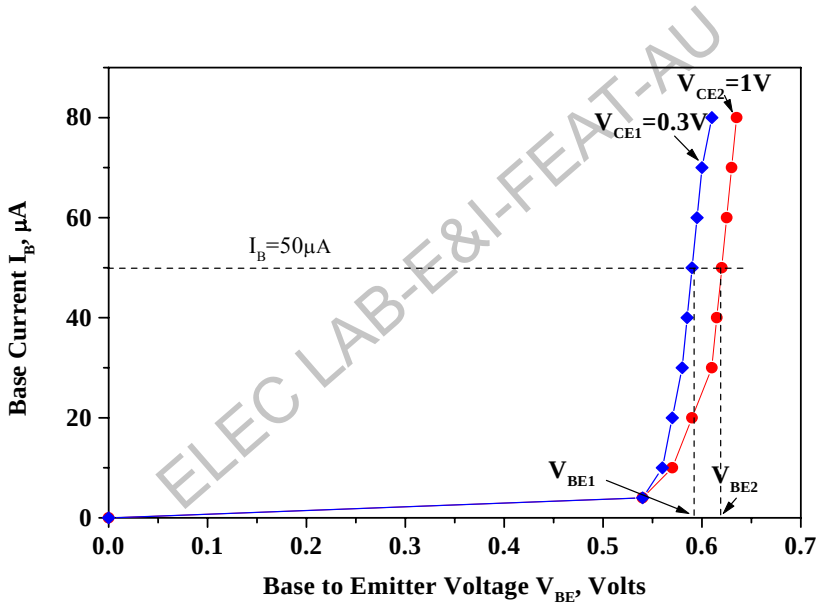


Fig.M2. I_B versus V_{BE} characteristics of given BJT

3. Mark the points $V_{BE1}, V_{BE2}, V_{CE1}, V_{CE2}$ as shown in the Fig.M2 and note down the values.
4. $\Delta V_{BE} = V_{BE2} - V_{BE1}$ and $\Delta V_{CE} = V_{CE2} - V_{CE1}$.
5. Calculate the reverse voltage transfer ratio of the given transistor using the formula $h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}$.

Table 1. Input Characteristics of the given Transistor

V_{CE} =1V		V_{CE} =0.3V	
V_{BE} (V)	I_B (μA)	V_{BE} (V)	I_B (μA)
0	0	0	0
0.54	4	0.54	4
0.57	10	0.56	10
0.59	20	0.57	20
0.61	30	0.58	30
0.615	40	0.585	40
0.62	50	0.59	50
0.625	60	0.595	60
0.63	70	0.6	70
0.635	80	0.61	80

Table2. Output Characteristics of the given Transistor

I_B =30 μA		I_B = 50 μA	
V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)
0	0	0	0
0.5	2	0.5	3.1
1	2.25	1	3.2
2	2.35	2	3.225
3	2.4	3	3.25
4	2.425	4	3.275
5	2.45	5	3.3
6	2.475	6	3.325
7	2.5	7	3.35
8	2.525	8	3.375

Determination of h_{fe} :

1. The measured data of the output characteristics using circuit shown in Fig.8 are given in Table2.
2. Draw the I_C versus V_{CE} characteristics as shown in the model graph given as Fig.M3 for two different values of I_B.

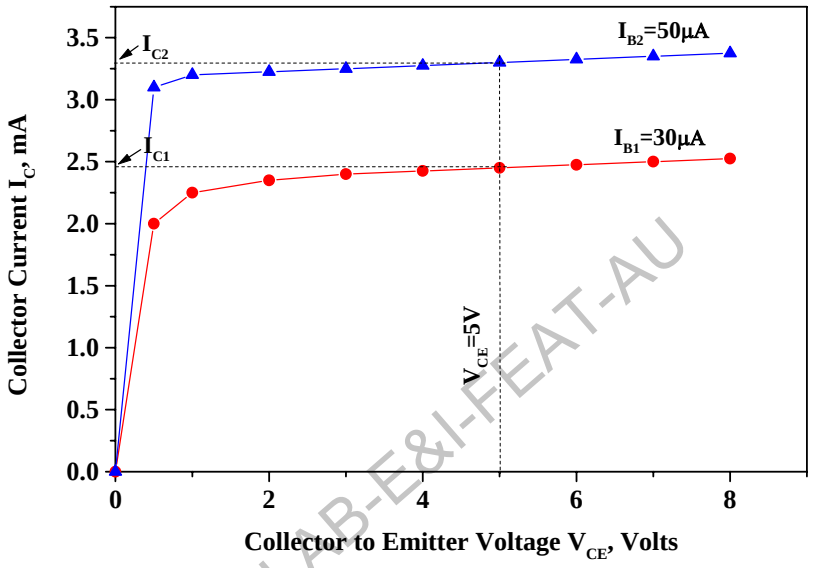


Fig.M3 I_C versus V_{CE} characteristics of given BJT

3. Mark the points $I_{B1}, I_{B2}, I_{C1}, I_{C2}$ as shown in the Fig.M3 and note down the values.
4. $\Delta I_B = I_{B2} - I_{B1}$ and $\Delta I_C = I_{C2} - I_{C1}$
5. Calculate the a.c forward current gain of the given transistor using the formula $h_{fe} = \frac{\Delta I_C}{\Delta I_B}$.

Determination of h_{oe} :

1. The measured data of the output characteristics are given in Table2.
2. Draw the I_C versus V_{CE} characteristics as shown in the model graph given as Fig.M4.

Table 3. Frequency Response characteristics of the given Amplifier

$V_{in} = 20mV$

S.No	Frequency (Hz)	Output Voltage V_o (Volts)	Voltage Gain Vo / Vin	Gain in dB 20 log (Vo/Vin)
1	20			
2	40			
3	60			
4	80			
5	100			
6	200			
7	400			
8	600			
9	800			
10	1000			
11	2000			
12	4000			
13	6000			
14	8000			
15	10000			
16	20000			
17	40000			
18	60000			
19	80000			
20	100k			
21	200k			

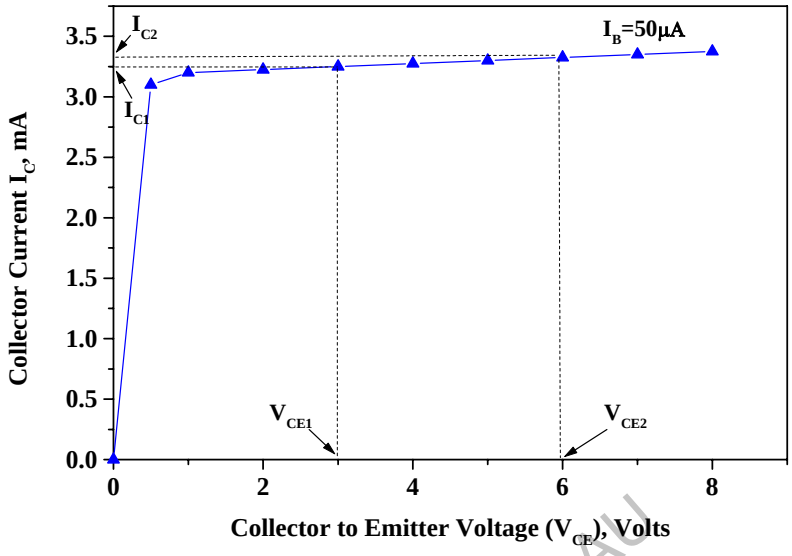


Fig.M4 I_C versus V_{CE} characteristics of given BJT

3. Mark the points I_{C1}, I_{C2}, V_{CE1} and V_{CE2} as shown in the Fig.M4 and note down the values.
4. $\Delta I_C = I_{C2} - I_{C1}$ and $\Delta V_{CE} = V_{CE2} - V_{CE1}$
5. Calculate the a.c output conductance of the given transistor using the formula

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}$$

Estimation of the analytical voltage gain of the given amplifier circuit

1. The amplifier for which the analytical voltage gain is to be estimated is given in Fig.9.
2. The equivalent circuit of the given transistor amplifier can be drawn as shown in Fig.10 using the hybrid equivalent model obtained in the previous sections.
3. The theoretical mid band voltage gain of the amplifier can be calculated using the formula

$$A_V = \frac{h_{fe} \times R_L'}{h_{ie} + \left(h_{ie}.h_{oe} - h_{re}.h_{fe}\right)R_L'}$$

Experimental measurement of the mid band voltage gain

1. Give the connections as per the circuit diagram shown in Fig.9.
2. Set the input voltage as 20mV in the signal generator.
3. Vary the input frequency from 20Hzto 200kHz and note down the output voltages.
4. Calculate the gain in dB using formula $20\log(V_o / V_{in})$ and plot the gain Vs frequency graph.
5. Compare the measured mid band gain with the analytically obtained mid band gain.

Result:

The h-parameters of the given transistor were obtained from the input and output characteristics. The h-parameter values obtained are summarized below.

Parameter	Measured Values	Unit
h_{ie}		Ohms
h_{re}		No dimension
h_{fe}		No dimension
h_{oe}		mho

Mid band voltage gain obtained by analytical method = ----------dB

Mid band voltage gain obtained experimentally = ----------dB

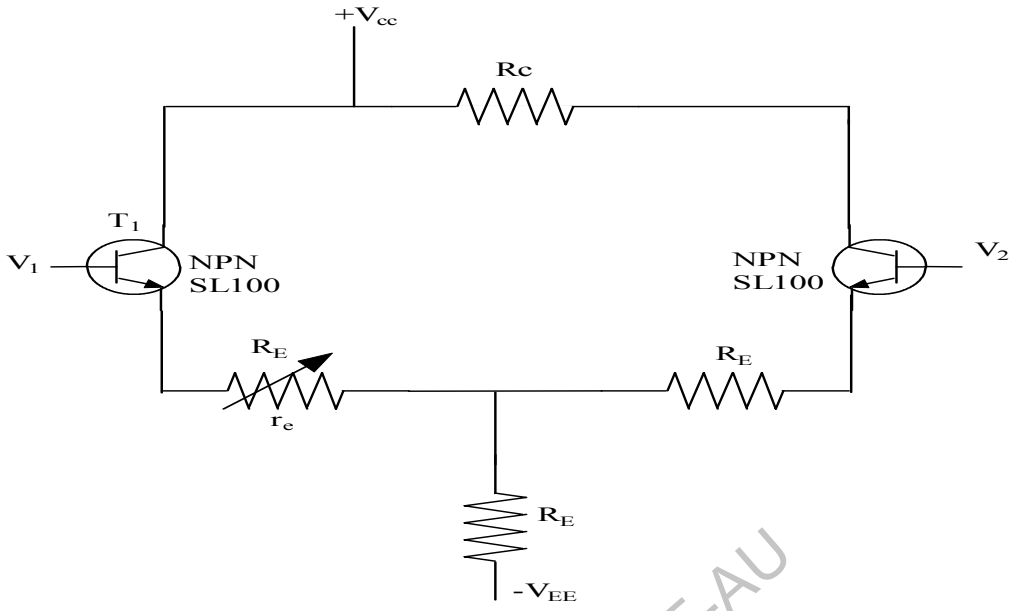


Fig.1 Double ended input single ended output Differential amplifier

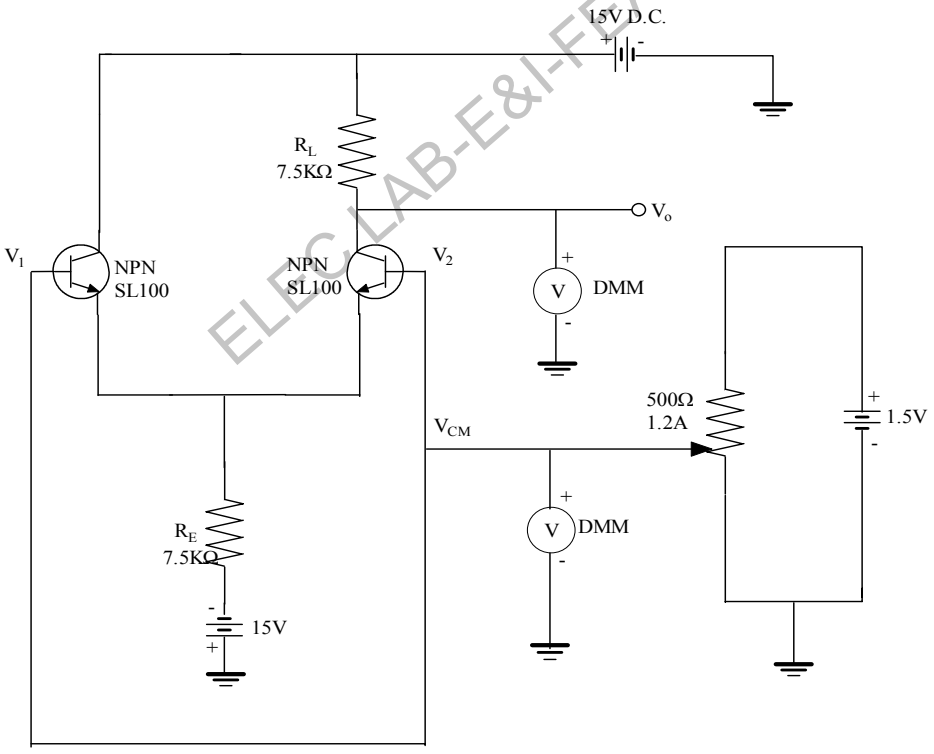


Fig.2 Experimental circuit diagram for estimation of Common mode gain

Exp. No:
Date :

MEASUREMENT OF DIFFERENTIAL MODE GAIN (A_D), COMMON MODE GAIN (A_{CM}) AND CMRR OF BJT DIFFERENTIAL AMPLIFIER

Aim

(i) To construct a BJT differential amplifier and to estimate its theoretical differential mode gain (A_d), common mode gain (A_{cm}) and CMRR.

(ii) To conduct suitable experiments and measure the practical differential mode gain (A_d), common mode gain (A_{cm}) and CMRR and compare them with the theoretical values.

Theory

A differential amplifier is an electronic circuit which amplifies the difference between its two input signals while rejecting any signal that the two inputs have in common.

Let V_1 and V_2 be the two input voltages then

Differential mode signal $V_d = V_1 - V_2$

Common mode signal $V_{cm} = \frac{V_1 + V_2}{2}$

Differential mode gain $A_d = \frac{V_{od}}{V_d}$ where V_{od} is the output when $V_{cm} = 0$

Common mode gain $A_{cm} = \frac{V_{ocm}}{V_{cm}}$ where V_{ocm} is the output when $V_d = 0$

Common Mode Rejection Ratio (CMRR) $= \frac{A_d}{A_{cm}}$

CMRR is a good indicator of the ability of the differential amplifier to reject the common mode input signal while amplifying the differential mode input signals.

Common Mode Rejection Ratio (CMRR) in dB $= 20 \log \left[\frac{A_d}{A_{cm}} \right]$

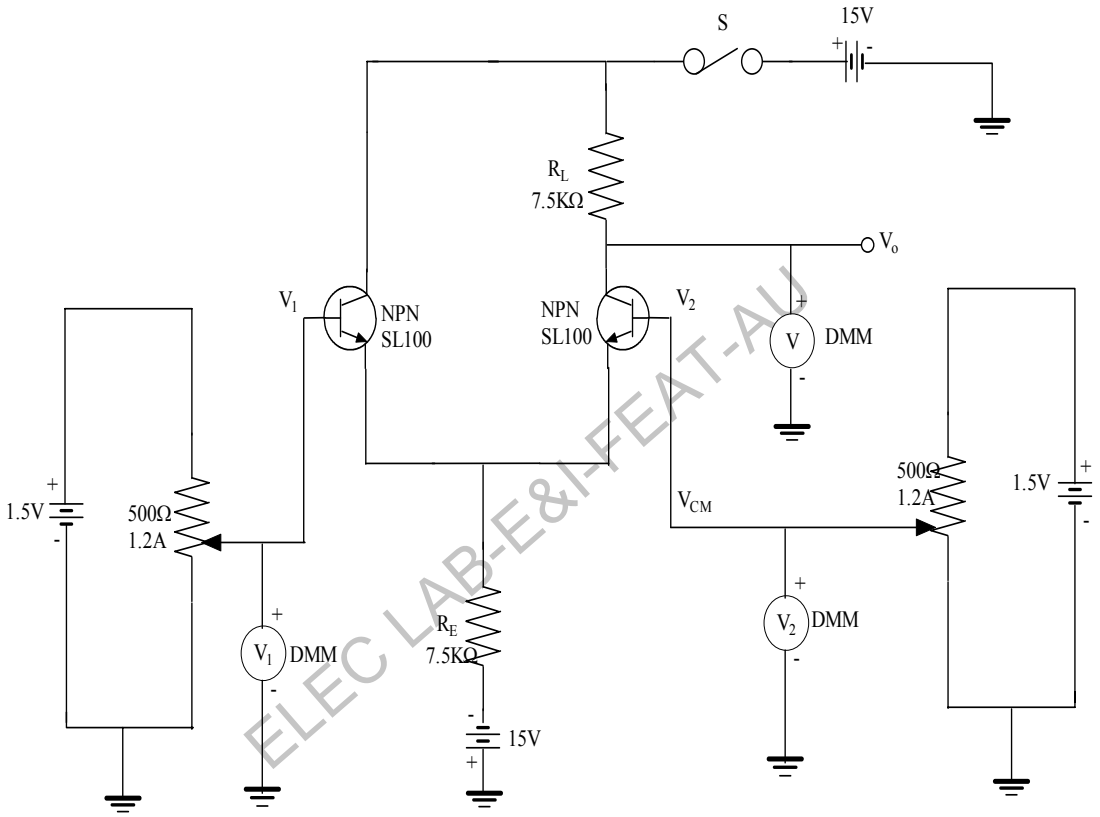


Fig.3 Experimental circuit diagram for estimation of differential mode gain

Fig.1 shows the most practical and widely used form of differential amplifier.This is called doubled ended input since it accepts differential inputs. But the output is not differential but is taken with respect to the ground. Therefore, the output is single ended. This has many applications because it can drive single ended loads like Common Emitter amplifiers, emitter follower etc. This type of differential amplifier is useful as the input stage for most of the high gain amplifiers. By theoretical analysis, it can be proved that

$$A_d \approx \frac{R_c}{2r_e}$$

$$A_{cm} \approx \frac{R_c}{2R_E + r_e}$$

where r_e = ac emitter resistance

$$= \frac{25mv}{I_c} \quad \text{where } I_c \text{ in mA}$$

Theoretical calculation of A_d, A_{cm} and CMRR:

$R_C = R_E = 7.5\ \text{k}\Omega$

$r_e = \frac{25mv}{I_c} = 25\ \Omega$ if $I_c = 1\text{mA}$.

$$A_d \approx \frac{R_c}{2r_e}$$

$$= \frac{7500}{2 \times 25} = 150$$

$$A_{cm} \approx \frac{R_c}{2R_E + r_e}$$

$$= \frac{7.5k}{2 \times 7.5k} = 0.5$$

$$CMMR = \frac{A_d}{A_{cm}} = \frac{150}{0.5} = 300; \text{ CMRR in dB} = 20\log\left[\frac{A_d}{A_{cm}}\right] = 20\log[300] = 49.5\,\text{dB}$$

Table 1. Estimation of common mode gain

S.No	$V_1 = V_2$ (V)	Measured V_o (V)	Actual V_{ocm} (V)	$V_{cm} = \frac{V_1 + V_2}{2}$ (V)	$A_{cm} = \frac{Actual V_{ocm}}{V_{cm}}$
1	0				
2	0.25				
3	0.5				
4	0.75				
5	1				
6	1.25				

Mean A_{cm} =…….

Table 2. Estimation of differential mode gain

S.No	V_1 (V)	V_2 (V)	$V_d = V_1 - V_2$ (V)	Measured V_o (V)	Actual V_{od} (V)	$V_{cm} = \frac{V_1 + V_2}{2}$ (V)	$A_d = \frac{Actual V_{od}}{V_d}$
1	0	0					
2	0.005	-0.005					
3	0.01	-0.01					
4	0.015	-0.015					
5	0.02	-0.02					
6	-0.005	0.005					
7	-0.01	0.01					
8	-0.015	0.015					
9	-0.02	0.02					
10	-0.025	0.025					

Mean A_d =…….

Procedure

Experimental estimation of common mode gain (A_{cm})

1. Give connections are as per the circuit diagram shown in Fig.2.
2. Note down the measured output voltages (V_o) for various common mode input voltages (V_{cm}) in the Table 1.
3. Calculate the actual common mode output voltage (V_{ocm}) by subtracting the measured output voltage V_o when the V_{cm}=0V.
4. Estimate the common mode gain (A_{cm}) using the formulae $A_{cm} = \frac{ActualV_{ocm}}{V_{cm}}$.
5. Calculate the mean A_{cm}.

Experimental estimation of differential mode gain (A_d)

1. Give connections are as per the circuit diagram shown in Fig.3.
2. Note down the measured output voltages (V_o) for various input voltages V_1 and V_2 in the Table 2.
3. Calculate the actual differential mode output voltage (V_{od}) by subtracting the measured output voltage V_o when V_1 and V_2 were set to 0V.
4. Estimate the differential mode gain (A_d) using the formulae $A_d = \frac{ActaualV_{od}}{V_d}$.
5. Calculate the mean A_d.

$$CMMR = \frac{A_d}{A_{cm}}$$

Result

For the given BJT differential amplifier differential mode gain , common mode gain and CMMR are theoretically calculated. By conducting experiments on the given BJT differential amplifier, the same parameters were practically measured. The results are tabulated as follows:

	Differential mode gain (A_d)	**Common mode gain (A_{cm})**	**CMRR in dB**
Theoretical	150	0.5	49.5
Experimental			

The experimental values are matching closely with the theoretical values.

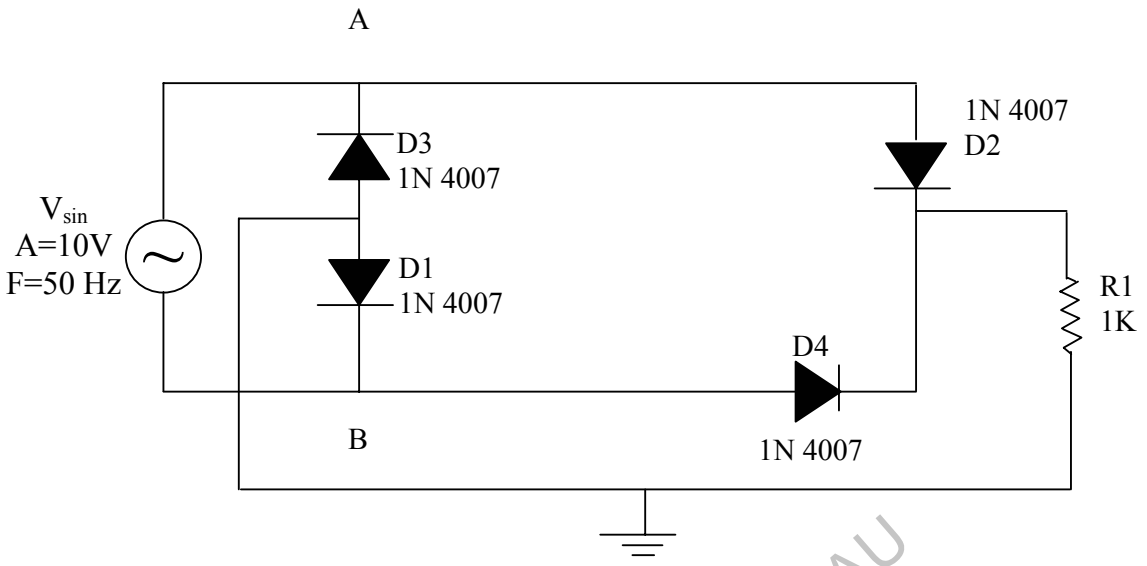


Fig.1 Circuit diagram of a Bridge rectifier with resistive load

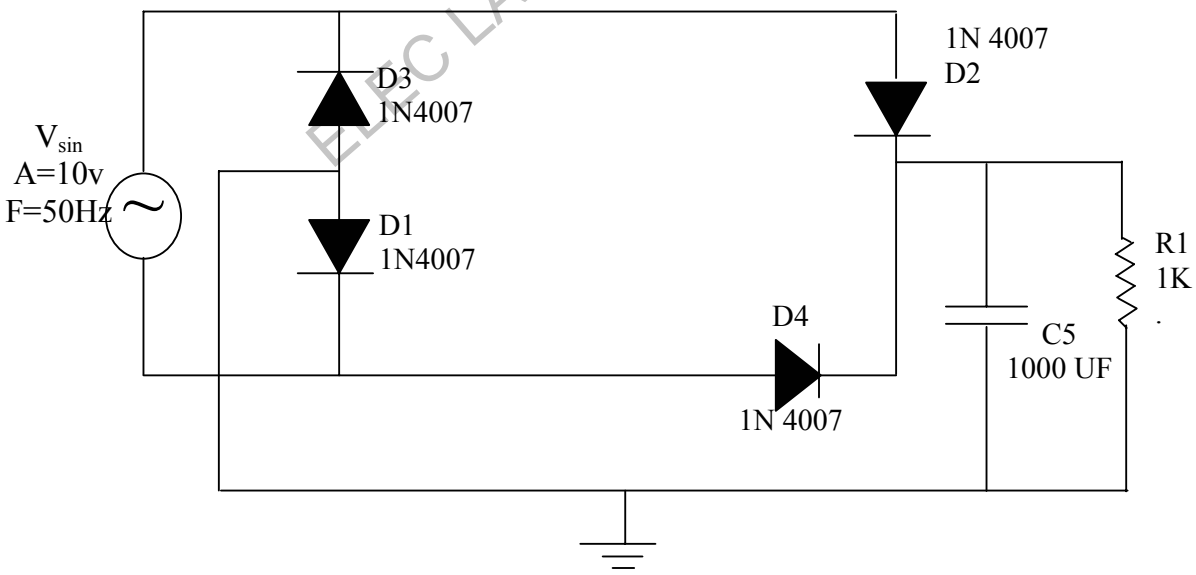


Fig.2 Circuit diagram of a Bridge rectifier with resistive load and capacitor filter

Exp. No:
Date :

SIMULATION OF FULL WAVE BRIDGE RECTIFIER WITH AND WITHOUT FILTER USING ORCAD SOFTWARE

Aim

To simulate the function of a full-wave bridge rectifier with and without filter using ORCAD software.

Apparatus Required

PC loaded with ORCAD software.

Theory

The circuit diagram of a Bridge rectifier with resistive load is shown in Fig.1. A rectifier is an electronic circuit which converts a.c. voltage into a pulsating d.c. voltage. During the positive half cycle of a.c supply if point marked **A** becomes positive and point **B** becomes negative, the voltages on the anode and cathode of four diodes are

i. Anode of diode D2 is positive with respect to cathode

ii. Anode of diode D1 is positive with respect to cathode

iii. Anode of diode D4 is negative with respect to cathode

iv. Anode of diode D3 is negative with respect to cathode

The diode which has its anode positive with respect to cathode is forward biased. Therefore, only diodes D2 and D_1 will conduct. These two diodes will be in series through load.

During the negative half cycle of a.c supply, point **A** becomes negative and point **B** becomes positive. The voltages on the anode and cathode of four diodes are

i. Anode of diode D_4 is positive with respect to cathode

ii. Anode of diode D_3 is positive with respect to cathode

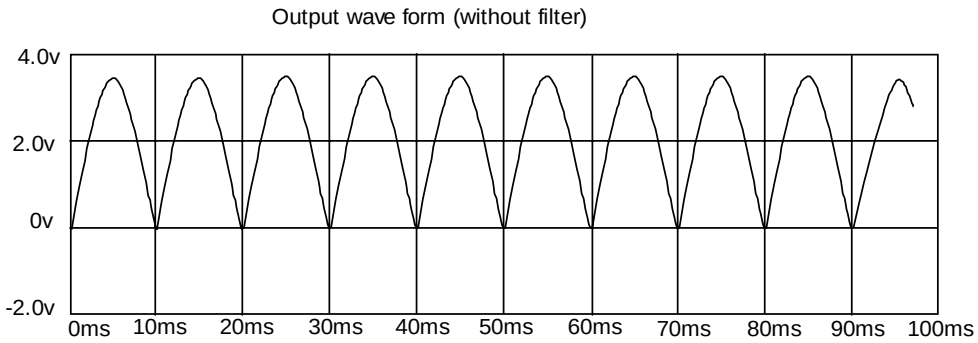


Fig.3 Load voltage for resistive load

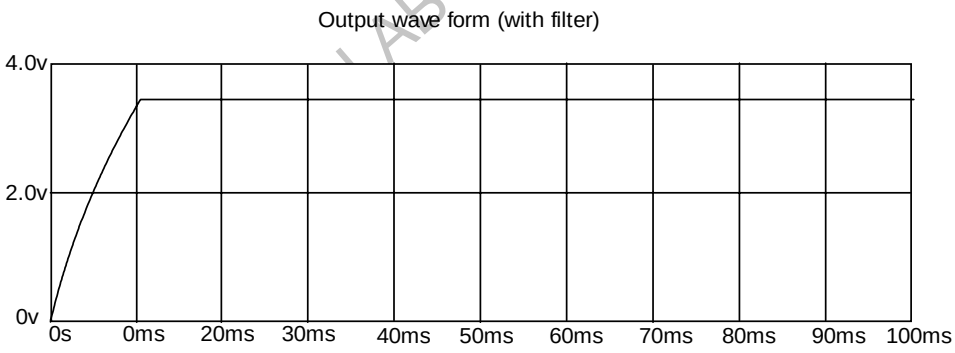


Fig.4 Load voltage for resistive load with capacitor filter

iii. Anode of diode D_2 is negative with respect to cathode

iv. Anode of diode D_1 is negative with respect to cathode

During the negative half cycle of a.c supply only diodes D_4 and D_3 will conduct. The conventional current flow is in the same direction as that of the previous half cycle of a.c supply and therefore the load voltage is pulsating d.c in nature.

When a filter capacitor is connected across the load as shown in Fig. 2, the a.c. components in the pulsating d.c are filtered and therefore an almost constant d.c voltage is obtained.

Simulation Procedure

1. **To open PSPICE ORCAD**: Go to programs in start menu and select ORCAD capture.

2. **To open a new project**: Select File option in the main men. Then select new. Another pop-up window appears in the select project option. Now type your file name and select analog or mixed A/D in the window that appears and click at OK.

   A window will appear, there select create Blank Project and enter. Now a new schematic page will open up.

3. **To place the components:** Select parts icon (second icon from the top) in the tool palette (right side of the screen) or select place option in the main menu, then select part in the pull down menu or press shift +P

4. **To select the required components from the components library:** Select the library listed in the library window, a list of components available in that library will be displayed in the list window there select the appropriate component. The component (part) name will appear in the part window and the circuit symbol will appear in the display box then click OK and place them in the schematic page.

5. **To wire the components:** Select wire (third icon from the top) in the tool palette or select place option in main menu, select wire in the pull down menu. A pointer cursor appears, click and drag to wire the components.

6. **To simulate the circuit:** Select PSPICE in main menu, select new simulation profile give a file name and click at create.

A window will appear on which enter the voltage probe, differential probe etc., from the tool bar and place them in the required position in the circuits.

Now again select PSPICE option in the main menu and select Run. Observe the load voltage waveforms for both cases which will be as shown in Fig.3 and Fig.4.

Result:

The operation of full-wave bridge rectifier with and without filter was simulated using ORCAD software.

Exp. No:
Date :

SIMULATION OF COMPLEMENTARY SYMMETRY POWER AMPLIFIER USING ORCAD SOFTWARE

Aim

To simulate the function of complementary symmetry power amplifier with R load using ORCAD software.

Apparatus Required

PC loaded with ORCAD software.

Theory

Fig. (1) shows the circuit diagram of complementary symmetry power amplifier. The diodes D1 and D2 are of the same type and R1=R2. Since both diodes are forward biased they help us to maintain +0.6V at base 1 and -0.6 V at base 2 under zero signal condition. Therefore, it is class AB operation. This helps us to minimize cross over distortion.

The operation of the amplifier for an a.c input voltage can be explained as follows: During positive half cycle of the a.c input voltage or when the signal is positive, the transistor Q1 is driven to active region and transistor Q2 is driven to cut off region. This is illustrated in Fig.2. The circuit operates as a common collector amplifier or emitter follower with voltage gain almost equal to one. This implies that the entire input appears across the load.

In the negative half cycle or when the input signal turns negative, the transistor Q2 is driven to active region and Q1 is driven to cut off region. This is illustrated in Fig.3. Again the PNP transistor operates as an emitter follower and the entire input appears across the load.

Thus in one full cycle, the NPN transistor conducts during positive half cycle and PNP transistor conducts during negative half cycle. Thus the output will be

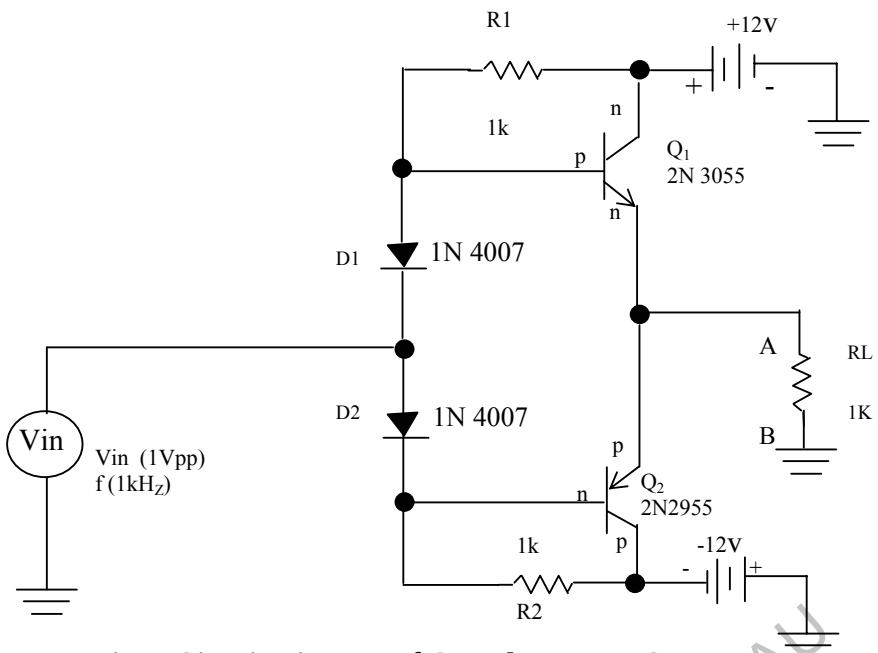


Fig 1: Circuit Diagram of Complementary Symmetry Power Amplifier

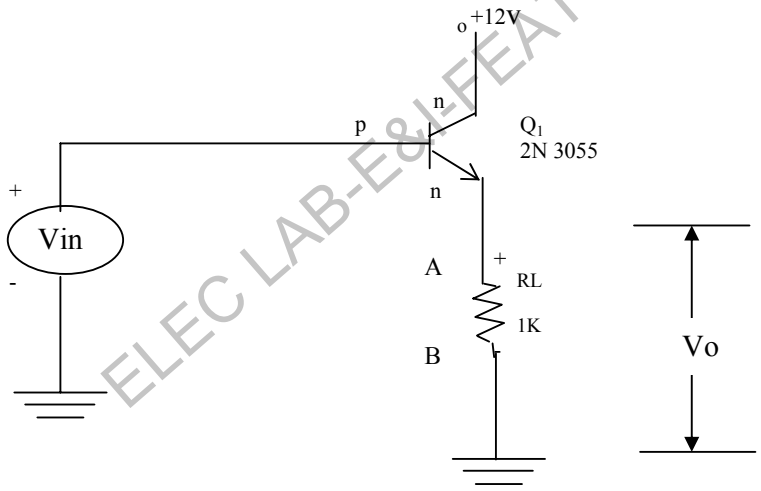


Fig.2 Circuit operation during positive half cycle of the a.c signal

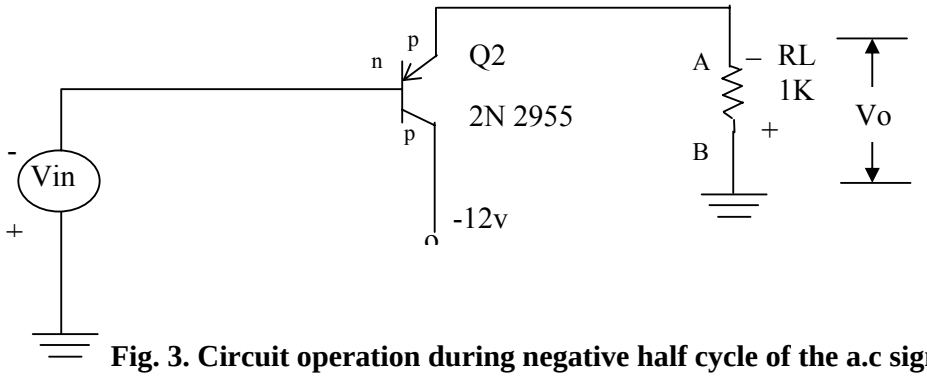


Fig. 3. Circuit operation during negative half cycle of the a.c signal

available in both half cycles. But the direction of the current differs in both half cycles as shown in Fig. 2 and Fig.3. The load current flows in from A to B in the positive half cycle and it flows from B to A in negative half cycle.

Procedure

1. **To open PSPICE ORCAD**: Go to programs in start menu and select ORCAD capture.

2. **To open a new project**: Select File option in the main menu, then select new, another pop-up window appears in that select project. Now type your file name and select analog or mixed A/D in the window that appears and click at OK.

   A window will appear, there select create Blank Project and enter. Now a new schematic page will open up.

3. **To place the components:** Select parts icon (second icon from the top) in the tool palette (right side of the screen) or select place option in the main menu, then select part in the pull down menu or press shift +P

4. **To select the required components from the components library:** Select the library listed in the library window, a list of components available in that library will be displayed in the list window there select the appropriate component. The component (part) name will appear in the part window and the circuit symbol will appear in the display box then click OK and place them in the schematic page.

5. **To wire the components:** Select wire (third icon from the top) in the tool palette or select place option in main menu, select wire in the pull down menu. A pointer cursor appears, click and drag to wire the components.

6. **To simulate the circuit:** Select PSPICE in main menu, select new simulation profile give a file name and click at create.

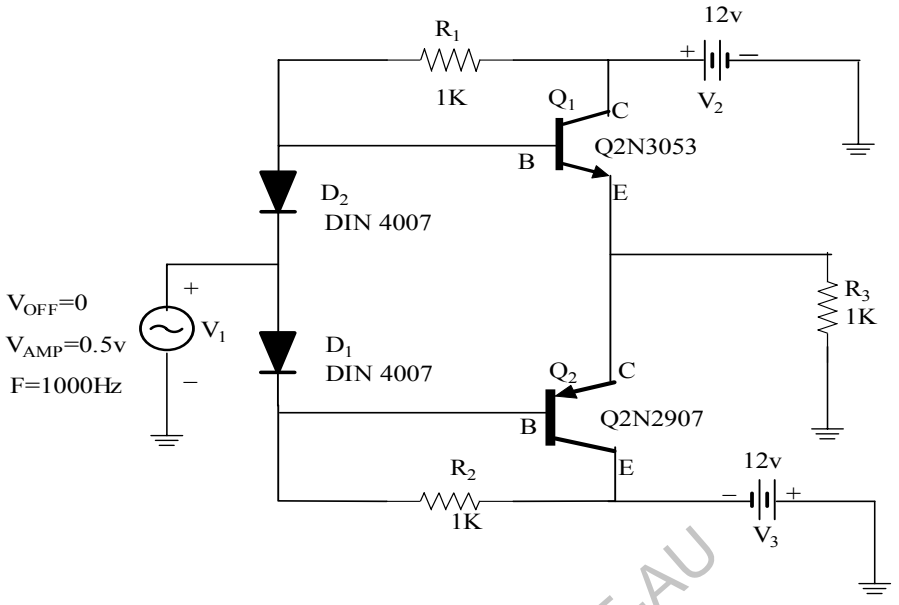


Fig.4 Simulation Circuit diagram of complementary symmetry power amplifier

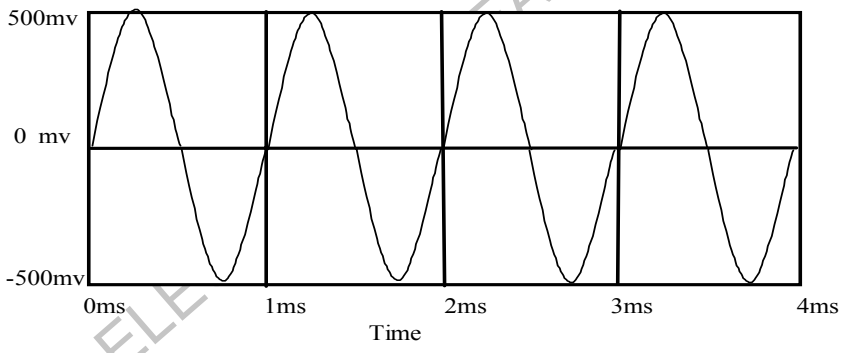


Fig.5 Input (voltage) signal

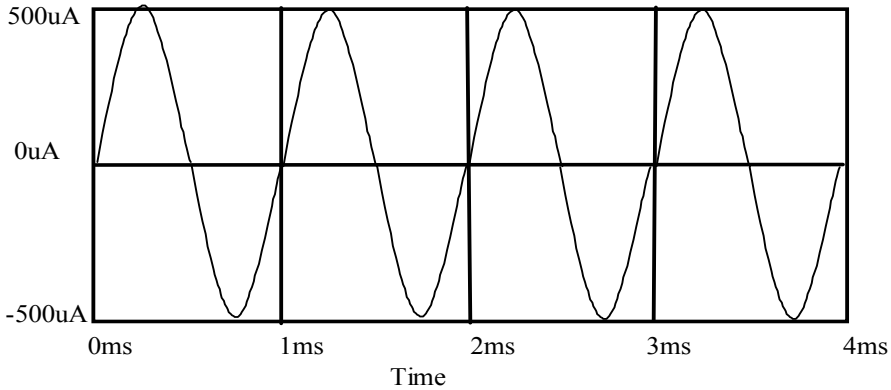


Fig.6 Output (load) current

A window will appear on which enter the voltage probe, differential probe etc., from the tool bar and place them in the required position in the circuits.

Now again select PSPICE option in the main menu, select Run. Observe the waveforms of input voltage and load current that will resemble the waveforms shown in Fig.5 and Fig.6.

Result

The operation of complementary Symmetry power amplifier with R load is simulated by using ORCAD software and output waveforms are observed.

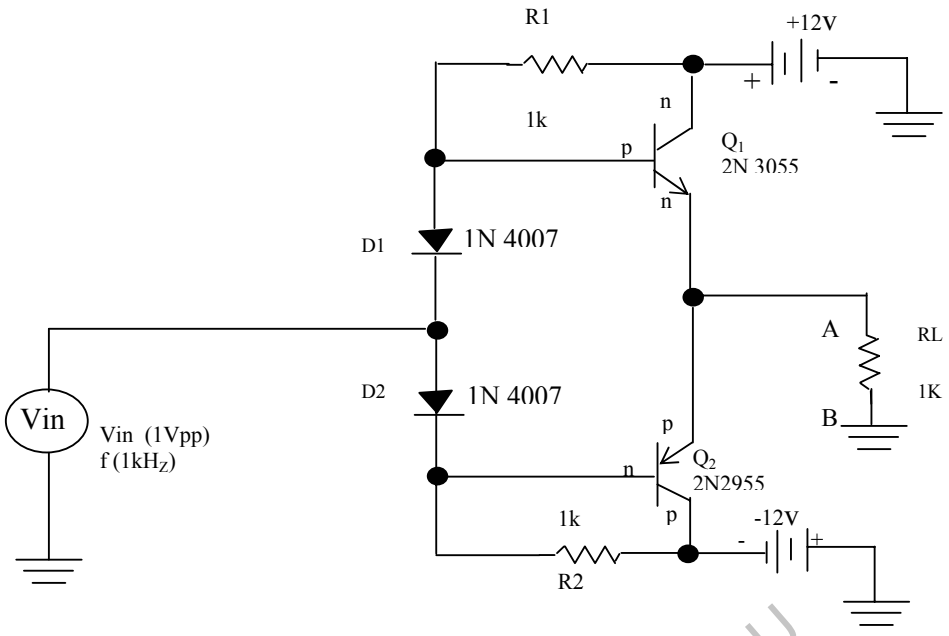


Fig 1: Circuit Diagram of Complementary Symmetry Power Amplifier

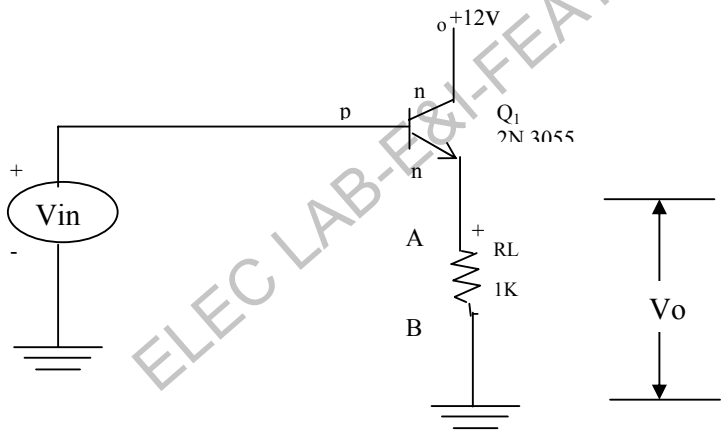


Fig.2 Circuit operation during positive half cycle of the a.c signal

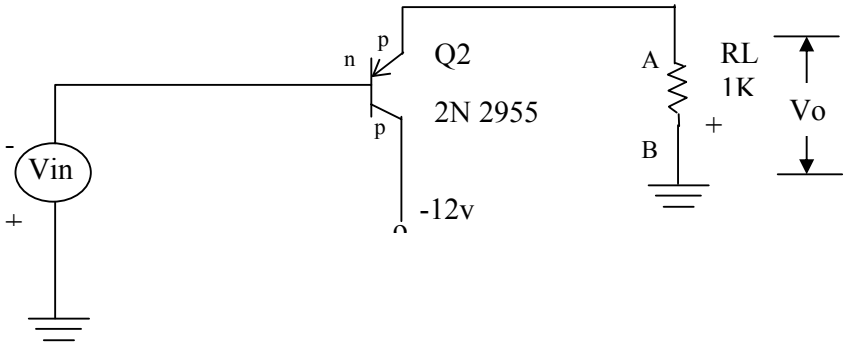


Fig. 3. Circuit operation during negative half cycle of the a.c signal

Exp. No:
Date :

COMPLEMENTARY SYMMETRY POWER AMPLIFIER

ANALYSIS AND DIRECTION CONTROL OF D.C MOTOR USING COMPLEMENTARY SYMMETRY POWER AMPLIFIER

Aim:

(i) To study the working of a complementary symmetry power amplifier

(ii) To drive a 12V DC motor using complementary symmetry power amplifier

Theory:

Fig. (1) shows the circuit diagram of complementary symmetry power amplifier. The diodes D1 and D2 are of the same type and R1=R2. Since both diodes are forward biased they help us to maintain +0.6V at base 1 and -0.6 V at base 2 under zero signal condition. Therefore, it is class AB operation. This helps us to minimize cross over distortion.

The operation of the amplifier for an a.c input voltage can be explained as follows: During positive half cycle of the a.c input voltage or when the signal is positive, the transistor Q1 is driven to active region and transistor Q2 is driven to cut off region. This is illustrated in Fig.2. The circuit operates as a common collector amplifier or emitter follower with voltage gain almost equal to one. This implies that the entire input appears across the load.

In the negative half cycle or when the input signal turns negative, the transistor Q2 is driven to active region and Q1 is driven to cut off region. This is illustrated in Fig.3. Again the PNP transistor operates as an emitter follower and the entire input appears across the load.

Thus in one full cycle, the NPN transistor conducts during positive half cycle and PNP transistor conducts during negative half cycle. Thus the output will be available in both half cycles. But the direction of the current differs in both half cycles

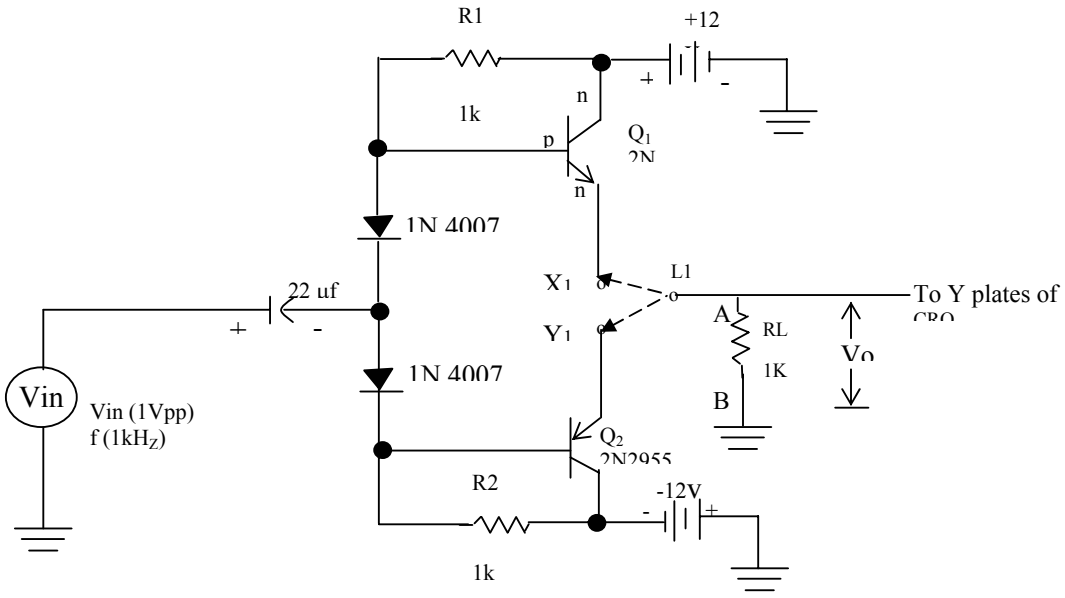


Fig. 4. Experimental circuit diagram for a resistive load

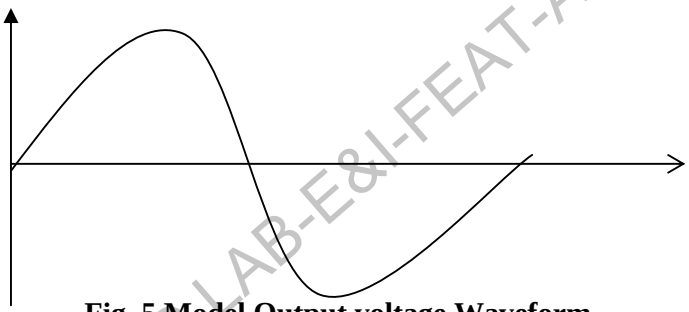


Fig. 5 Model Output voltage Waveform

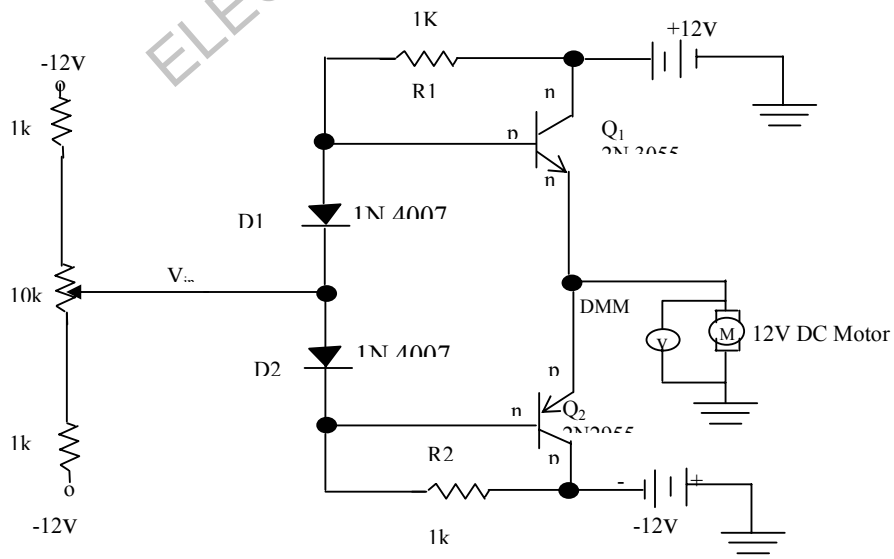


Fig. 6 Practical Circuit Diagram for driving motor load

as shown in Fig. 2 and Fig.3. The load current flows in from A to B in the positive half cycle and it flows from B to A in negative half cycle.

Experimental Procedure:

Connect up and energise the circuit as shown in Fig. 4.

1. Set V_{in} = 1 V peak to peak and set the frequency to 1000 Hz.
2. Connect X_1 with L_1 and observe the waveform of output voltage (V_o). In this case you get only positive half cycles in the output. This indicates that the NPN transistor is responsible for the amplification of the positive input.
3. Disconnect X_1 from L_1 and now connect Y_1 to L_1 and observe the waveform of output voltage (V_o). In this case you get only negative half cycles in the output. This indicates that the PNP transistor is responsible for the amplification of the positive input.
4. Then connect X1, Y_1 and L_1 all together and observe waveform of the output voltage (V_o). You will get a waveform as shown in Fig. 5.
5. The gain of the amplifier can be estimated using $A_V = \frac{V_{o(p-p)}}{V_{in(p-p)}}$.

Direction control of D.C. Motor:

1. Connect up and energise the circuit as shown in Fig.6. The potentiometer (10k POT) helps us to set any voltage between -10V to and +10V.
2. Connect the DC motor with its positive terminal at point A and its negative terminal at B in the place of R_L.
3. Switch on the power supply unit, gradually increase V_{in} up to +3V by adjusting the potentiometer and note down the direction of rotation of the motor shaft. Indicate your observations in the Table.
4. Increase V_{in} to + 6V DC and check if the speed increases.
5. Now reverse the polarity of V_{in} by adjusting the potentiometer and setting the input voltage at -3V and note down the direction of rotation of motor shaft.
6. Increase V_{in} to -6V DC and check if the speed increases. Indicate your observations in Table.1.

Table 1. Observation Table for Direction control of D.C motor

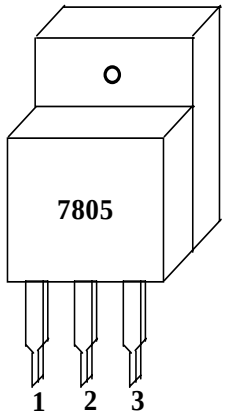
V_{in} (Volts)	V_o (Volts)	Direction of the shaft movement	Speed status
3			
4			
5			
6			
-3			
-4			
-5			
-6			

(Note CW if direction is clockwise or ACW if direction is Anti clockwise; Increase in speed should be indicated by an upward arrow)

Result:

The complementary symmetry power amplifier was studied and the gain of the amplifier is measured to be …….. The cross over distortion was found to be absent in this amplifier due to Class AB operation. The same amplifier was used to drive a DC motor load and control its direction. The performance of the complementary symmetry power amplifier was found to be satisfactory.

TO - 220 PLASTIC PACKAGE OF IC 7805



TYPICAL CIRCUIT CONNECTION FOR IC 7805

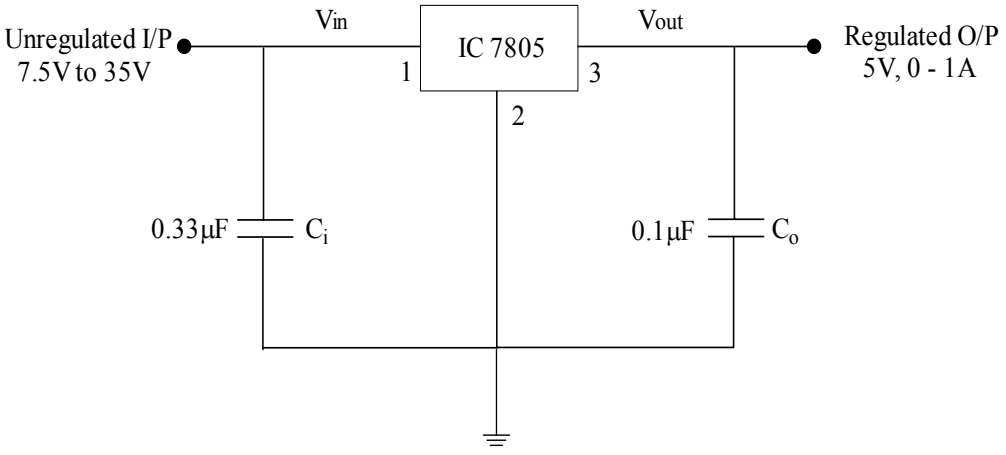


Fig. 1. Typical Circuit connection for IC 7805

Exp. No:
Date:

LINE AND LOAD REGULATION CHARACTERISTICS OF INTEGRATED CIRCUIT (IC) FIXED VOLTAGE REGULATOR

Aim:

To construct an integrated circuit fixed voltage regulator using 78XX series voltage regulator and study its line and voltage regulation characteristics.

Components Required:

Auto Transformer 1φ, 230V/270V	– 1 No.
Step down Transformer 1φ, 230V/15V`	– 1 No.
Diodes (BY 127)	– 4 Nos.
IC – 7805	– 1No.
Capacitor 1000μF, 0.1μF	– 1No.
Milli ammeter (0 - 100mA)	– 1 No.
Voltmeter (0 - 40V)	– 1 No.
Rheostat 3.6KΩ, 0.3A	– 1 No.

Specifications of IC 7805:

Output Voltage – 5V DC
Max. Input Voltage – 35V DC
Max. Output Current – 1A
IC 7805 is available in TO -220 plastic package

Theory:

A D.C voltage regulator is an electronic circuit designed to maintain a constant predetermined output voltage irrespective of fluctuation in line voltage and changes in load current. However, the input voltage must be more than the desired output voltage

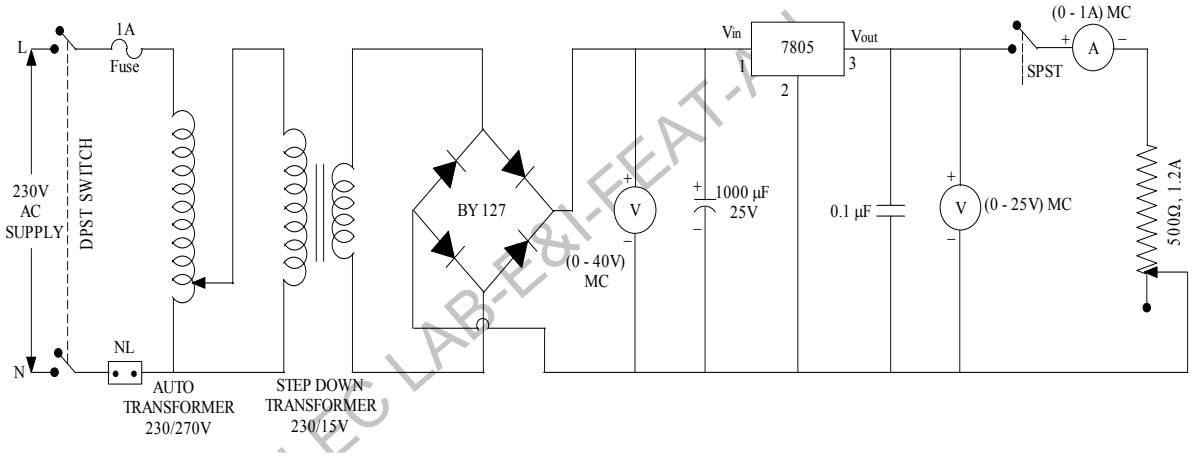


Fig.2 Experimental Circuit Diagram of IC Voltage Regulator

by at least the dropout voltage. The 78XX series of IC's provide three terminal positive voltage regulators with seven output voltage options as given in the Table 1.

Table 1. Various output voltage options available in 78XX series

TYPE	OUTPUT VOLTAGE (Volts)	MAX. INPUT VOLTAGE (Volts)
7805	5.0	35
7806	6.0	35
7808	8.0	35
7812	12.0	35
7815	15.0	35
7818	18.0	35
7824	24.0	40

IC 7805 provides a constant output voltage of 5 Volts for line (input voltage) and load (load current) variations. The proper operation requires a common ground between input and output voltage as shown in Fig.1. In addition, the difference between input and output voltages (Vin ~Vo) called **dropout** voltage must be typically 2V. The capacitor C_i filters out the effect of stray inductance in the input wires and is required if the regulators are located at appreciable distance from a power supply. Filter capacitor C_o may be used to improve the transient response of the regulator to sudden load current changes.

Procedure:

I. Line Regulation Characteristics:

A DC voltage regulator starts with an unregulated voltage source, V_{in}, and provide a regulated voltage of V_o. In a practical DC regulator, if the input voltage to the regulator changes (e.g., by amount ΔV_{in}), the output voltage will change (e.g., ΔV_o). Line regulation, S_v, describes how the voltage regulator hold its output voltage

Model graphs

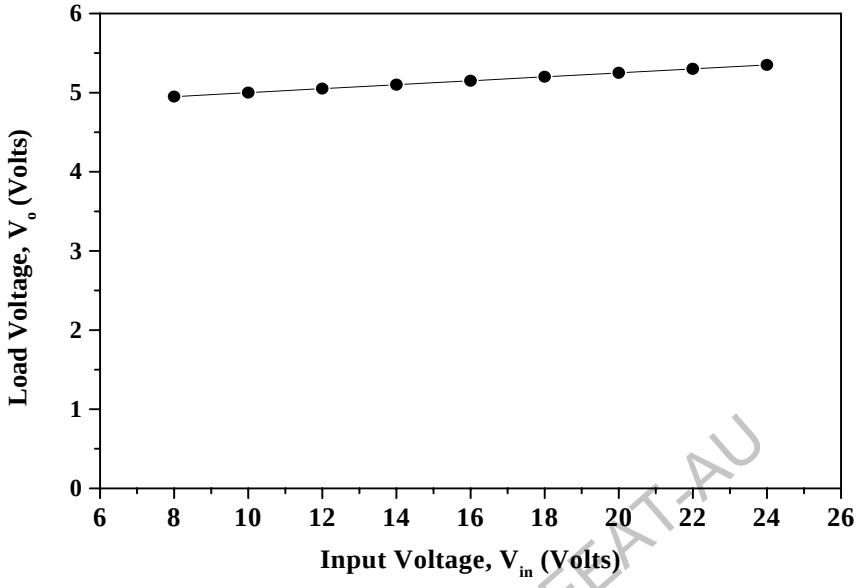


Fig.3 Line Regulation Characteristics (Model Graph)

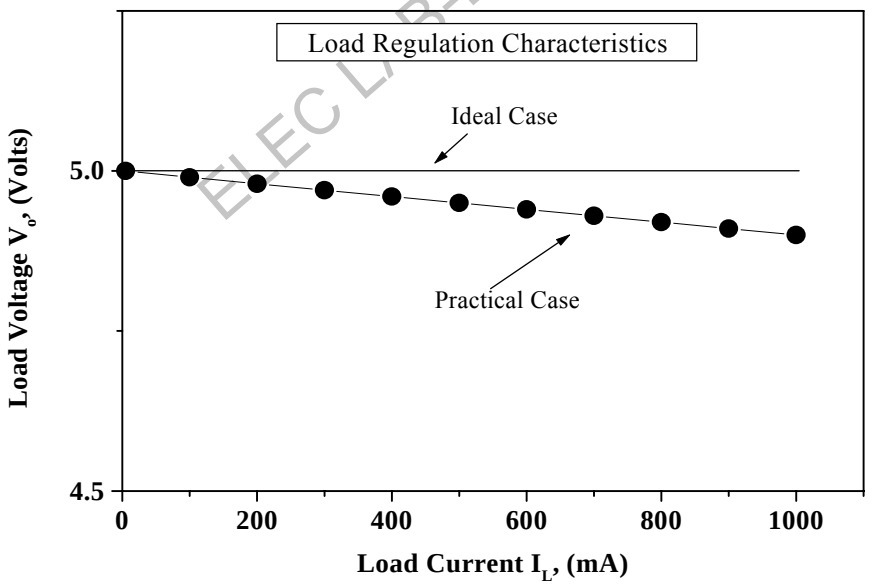


Fig.5 Load Regulation Characteristics (Model Graph)

constant when the input voltage changes, and is defined as $S_v = \frac{\Delta V_o}{\Delta V_{in}}$. Good regulators have small line regulation. The line regulation characteristics explain the ability of a voltage regulator to maintain a predetermined output voltage for variation in input voltage at a constant load. Therefore, it is important to maintain the load constant during this study.

1. Give the connections as per the circuit diagram shown in Fig. 2.
2. Now keep the unregulated input at 24V by increasing the auto transformer output voltage.
3. Now keep the load resistance value maximum and close the SPST switch. Set the load current to 500mA.
4. Now decrease the input voltage in steps of 2V and note down the corresponding input and output voltages in Table 1.
5. Obtain the line regulation characteristics by plotting the output voltage against the input voltage as shown in the model graph shown in Fig.3.
6. Calculate the line regulation factor S_v from the formulae

$$S_v = \frac{\Delta V_o}{\Delta V_{in}} \qquad mV/V$$

II. Load Regulation Characteristics:

In a practical voltage regulator, as the current drawn from the regulator (I_L is increased), the output voltage drops. This behavior can be modeled by replacing the voltage regulator with its Thevenin equivalent (See Fig.4). The Thevenin's resistance of the regulator is usually called the output resistance. From the circuit below, we have $R_o = \frac{V_{in} - V_o}{I_L}$. As more current is drawn from the regulator, the voltage drop across this internal resistance is increased and the output voltage is decreased.

Table 1. Line Regulation Characteristics
Load Current, I_L = 500mA

Input Voltage (V_{in}) (Volts)	**Load Voltage (V_o) (Volts)**	$S_v = \frac{\Delta V_o}{\Delta V_{in}}$
8		
10		
12		
14		
16		
18		
20		
22		
24		

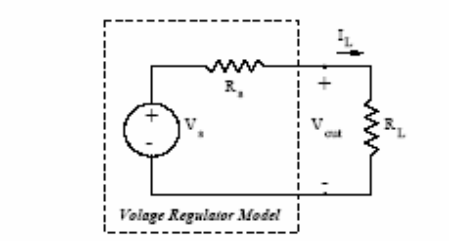


Fig.4. Thevenin's equivalent Circuit of the voltage regulator

The load regulation characteristics explain the ability of a voltage regulator to maintain a predetermined output voltage for variation in load current at a constant input voltage. Therefore, it is important to maintain the input voltage constant during this study.

1. Give the connections as per the circuit diagram shown in Fig. 2.
2. Now keep the load resistance value maximum and close the SPST switch.
3. Set the input voltage at pin 1 of 7805 at 15V.
4. Measure the output voltage at a load current of 5mA and note down in Table 2.
5. Repeat the measurements for a load current starting from 50 mA to 1000 mA at an interval of 50mA.
6. Obtain the load regulation characteristics by plotting the output voltage against the load current as shown in the model graph shown in Fig.5.
7. Calculate the output resistance (R_o) from the formulae

$$R_o = \frac{\Delta V_o}{\Delta I_L} \qquad mV / A$$

Precautions

1. The output voltage of the auto-transformer should not exceed 230V.
2. The input voltage applied to IC7805 should not exceed 35V.

Table 2. Load Regulation Characteristics

Input Voltage V_{in} = 15V

Load Current (I_L) (mA)	**Load Voltage (V_o) (Volts)**	$R_o = \frac{\Delta V_o}{\Delta I_L}$
5		
100		
200		
300		
400		
500		
600		
700		
800		
900		
1000		

Result:

A fixed voltage regulator was constructed and tested using IC 7805. The line regulation and load regulation characteristics were studied. The line regulation factor and output resistance were estimated.

The line regulation factor (S_v) is = ……

The output resistance (R_o) is = ……

Exp No:
Date:

DESIGN AND SIMULATION OF CLASS A AMPLIFIER USING ELECTRONIC WORK BENCH

Aim

To design a class-A amplifier using Bipolar Junction Transistor and to obtain its frequency response using electronic workbench circuit simulation software.

Theory

The class-A amplifier is, basically a common emitter amplifier as shown in Fig.1. In the class-A amplifier the transistor bias and amplitude of the input signal are such that the output current flows for the complete cycle (i.e. 360°) of the input signal. This condition is achieved by locating the Q-point somewhere near the centre of the load line. This leads to obtaining the maximum output signal. The operation of the amplifier is restricted to smaller central region of the load line, so that the circuit can operate in the linear region of the load line. The large signals may shift the Q-point into non-linear regions near saturation or cut-off and hence produce amplitude distortion. Since the amplifier operates over the linear region of the load line, therefore the output waveform is almost similar to the input waveform.

Design

The voltage divider biasing network is used in this amplifier

From the circuit,

$$V_{CC} = I_C R_C + V_{CE} + V_E$$
$$= I_C R_C + V_{CE} + I_C R_E$$

since I_B is very small, $I_C \approx I_E$

$$V_{CC} = V_{CE} + I_C R_C + I_E R_E$$
$$= V_{CE} + I_C (R_C + R_E)$$
$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E} \qquad (1)$$

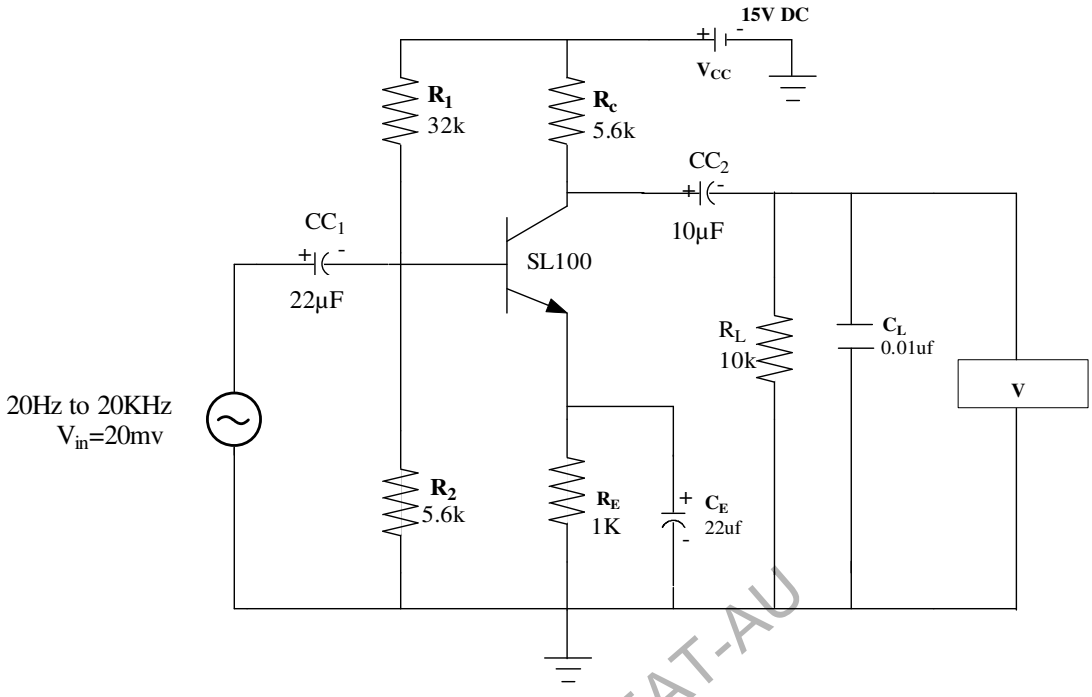


Fig.1. Class-A amplifier.

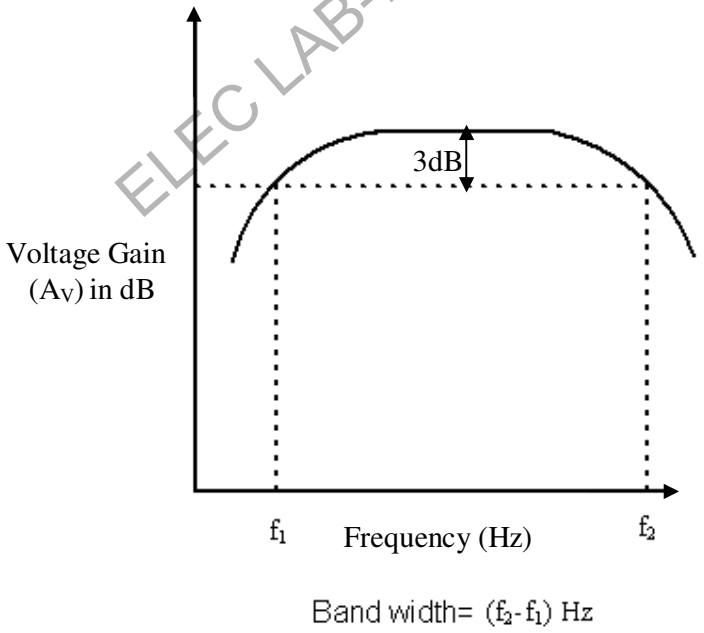


Fig.2. Model Graph

Design of R_C and R_E

Let us assume $V_{CC} = 15V$, $V_{CE} = 5V$, $I_C = 1.5mA$

Substituting the above values in equation (1)

$$1.5\times10^{-3} = \frac{(15-5)}{R_C + R_E}$$

$$R_C + R_E = 6.6k\Omega \qquad (2)$$

For better amplification, the voltage drop across R_C should be low.

Let us assume that the emitter voltage is one tenth of supply voltage.

$$V_E = \frac{V_{CC}}{10} = \frac{15}{10} = 1.5V$$

$$R_E = \frac{V_E}{I_E}$$

$$= \frac{1.5}{1.5\times10^{-3}}$$

$$= 1k\Omega$$

Hence $R_C = 6.6 - 1 = 5.6\ k\Omega$

Now,

$$V_{R2} = V_{BE} + V_E$$

$V_{BE} = 0.7V$ for silicon transistor

$V_{R2} = 2.2V$

$$I_1 = \frac{V_{CC}}{(R_1 + R_2)} \qquad (3)$$

$$\beta = \frac{I_C}{I_B}$$

As $\beta = 40$

$$I_B = \frac{I_C}{\beta} = \frac{1.5\times10^{-3}}{40}$$

$$= 0.0375mA$$

Design of Biasing Resistors R_1 and R_2

$$I_1 = 10 \times I_B$$
$$= 10 \times 0.0375 \times 10^{-3}$$
$$= 0.375\text{mA}$$

Substitute I_1 in equation (3)

$$R_1 + R_2 = \frac{V_{CC}}{I_1}$$
$$= \frac{15}{(0.375 \times 10^{-3})}$$
$$= 40\,\text{k}\Omega \qquad (4)$$

$$I_2 = I_1 - I_B = (0.375 - 0.0375)mA = 0.3375mA$$

$$R_2 = \frac{V_2}{I_2}$$
$$= \frac{2.2}{(0.3375 \times 10^{-3})}$$
$$= 6.51\text{k}\Omega$$

Substitute R_2 in equation (4)

$$R_1 + R_2 = 40\,\text{k}\Omega$$
$$R_1 = 40 - 6.5 = 33.5\text{k}\Omega$$

Design of C_{C1},C_{C2} and C_E

The signal is coupled to the base of the transistor through a capacitor C_{C1}. The purpose of this capacitor is to block dc so as not to disturb the bias conditions already established. The value of C_{C1} should be chosen, sufficiently large so that for wide signal frequencies of our interest it acts as a short circuit. Obviously, C_{C1} will cause the amplifier gain to drop at low frequencies and will cause the gain to be zero at dc.

The output signal voltage at the collector is coupled to a load resistance R_L through another coupling capacitance C_{C2}. Again C_{C2} should be chosen large in

order to act as a perfect coupler at all frequencies of interest. Let us assume R is 10 times greater than that of X_C,

$X_{C1} = 100\Omega$

$$100\Omega = \frac{1}{2\times\pi\times100\times C}$$

Therefore $C_{C1} \cong 22\mu F$

$X_{C2} = 0.1R$ (or) $0.1\times10 = 1\,k\Omega$.

$$X_{C2} = \frac{1}{2\Pi fc}$$

At the lowest frequency $1k\Omega = \frac{1}{2\times\pi\times20\times C}$

Therefore $C_{C2} = 7.96\mu F \approx 10\mu F$

The bypass capacitor C_E acts as by-pass to the amplified a.c. signal.

Let $X_E << R_E$

$$\frac{R_S}{X_{CS}} = 10$$

$$X_{CS} = \frac{R_E}{10} = \frac{1k\Omega}{10} = 100\Omega$$

$$C_E = \frac{1}{2\times3.14\times100\times100} \approx 22\mu F$$

.

Procedure

(1) Wire the circuit as per the circuit diagram shown in Fig.1. using electronic work bench software.
(2) Keep the input voltage at 20mV.
(3) Keeping the input voltage constant, vary the input frequency from 20 Hz to 20 kHz and note down the corresponding output voltage.
(4) Calculate the gain in dB using the formula given below

$$Gain = 20\log\left(\frac{V_O}{V_{in}}\right)$$

(5) Draw the frequency response curve and calculate the band width.

Tabulation

Input Voltage = 20 mV

Frequency (Hz)	**Output Voltage (Volts)**	**Voltage Gain = 20log(V_0/V_{in})**
20		
40		
60		
80		
100		
200		
400		
600		
800		
1k		
2k		
3k		
4k		
5k		
6k		
7k		
8k		
9k		
10k		
20k		
40k		
60k		
80k		
100k		
200k		

Result

Thus the class A amplifier is designed and its parameters have been estimated and tabulated below

Parameter	Theoretical Value	Measured Value	Unit
Voltage Gain			
Bandwidth			

Exercise

(1) What is class A amplifier?

(2) What is the use of bypass capacitor?

(3) What is the need for estimation of bandwidth?

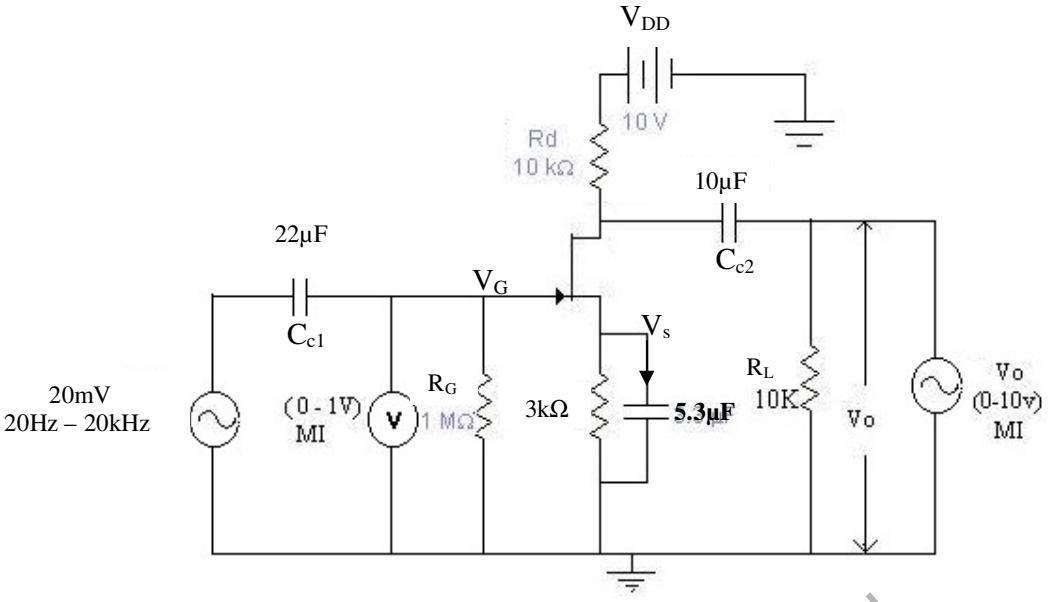
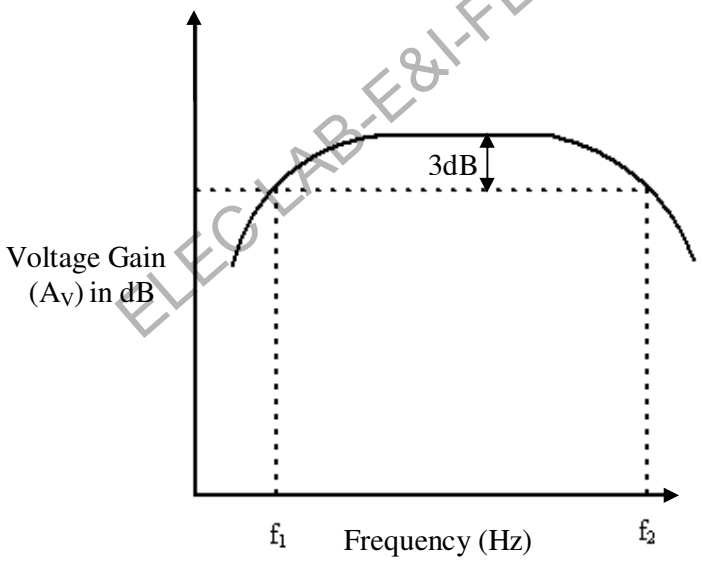


Fig.1. Common source FET Amplifier



Band width= (f_2-f_1) Hz

Fig.2. Model Graph

Exp. No:
Date:

DESIGN AND TESTING OF COMMON SOURCE FET AMPLIFIER

Aim

(i)To Design a common source FET amplifier
(ii)To study its frequency response characteristics

Theory

The circuit diagram of the common source amplifier is shown in Fig.1.The resistance R_G provides a path to ground for d.c. signals. Also the input resistance of the amplifier is determined by R_G and in this case 1MΩ. Since it establishes 0V at the gate, it is also called biasing resistor.

Capacitors C_{C1} and C_{C2} are used as coupling capacitors. Capacitor C_{C2} couples the a.c. signal to the load, whereas C_{C1} couples the input signal to the gate.

The resistor R_S connected in the source lead of the FET amplifier provides self biasing and thermal stability. This resistor should be adequately bypassed by bypass capacitor to avoid a degenerative effect for d.c. due to negative feedback.

$$V_S = I_D.R_S \quad \text{Therefore } V_{GS} = 0-I_DR_S = -I_DR_S$$

Signal generator is used to give the input signal from 20Hz - 20 kHz.

Circuit Description

A signal generator is used in audio frequency amplifier such as FET this should extend in the range of 20Hz to 20 kHz. Since this is the nominal frequency range to which the ear is sensitive.

FET is biased using a combination of fixed bias and self-bias. Though small gate current flows through R_G, this current increases with temperature its value imposes an upper limit to R_G. Otherwise the bias point of the FET becomes temperature dependent.

The signal is coupled to the gate of the FET through a capacitor C_{C1}. The purpose of this capacitor is to block dc so as not to disturb the bias conditions already established. The value of C_{C1} should be chosen, sufficiently large so that for wide signal frequencies of our interest it acts as a short circuit. Obviously, C_{C1} will cause the amplifier gain to drop at low frequencies and will cause the gain to be zero at dc.

The output signal voltage at the drain is coupled to a load resistance R_L through another coupling capacitance C_{C2} . Again C_{C2} should be chosen in order to act as a perfect coupler at all frequencies of interest.

Tabulation

Input Voltage (V_{in}) = 20mV

Frequency (Hz)	**Output Voltage (Volts)**	**Voltage Gain = 20log(V_0/V_{in})**
20		
40		
60		
80		
100		
200		
400		
600		
800		
1k		
2k		
3k		
4k		
5k		
6k		
7k		
8k		
9k		
10k		
20k		
40k		
60k		
80k		
100k		
200k		

$$X_{CS} = \frac{R_S}{10} = \frac{3k\Omega}{10} = 300\Omega$$

$$C_S = \frac{1}{2\times 3.14\times 100\times 300} = 5.307\mu F$$

Estimation of Voltage Gain

$$g_{mo} = \frac{2I_{DSS}}{V_P} = \frac{2\times 4mA}{6}$$

$$g_{mo} = 1.33m \text{ mho}$$

$$g_m = g_{mo}\times\left(1-\frac{V_{GS}}{V_P}\right)$$

$$= 1.33\times 10^{-3}\left(1-\frac{(-3)}{6}\right) = 1.33\times 10^{-3}\left(1+\frac{3}{6}\right) = 1.95\times 10^{-3}$$

$$A_V = g_m R_d = 19.5\times 10^{-3}\times 10k\Omega$$

$$A_V = 19.5$$

Design of C_{C1} and C_{C2}

$$X_{C1} = 0.1\times 5k\Omega = 500\Omega$$

$$C_{C1} = \frac{1}{2\times\Pi\times f\times X_{C1}} = \frac{1}{2\times\Pi\times 100\times 500} \approx 5\mu F$$

$$X_{C2} = \frac{R_D}{10}$$

$$C_{C2} = \frac{1}{2\times\Pi\times f\times X_{C2}} = \frac{1}{2\times\Pi\times 20\times 1000} \approx 10\mu F$$

Procedure

1. The input signal is given from a signal generator and the input voltage is maintained at 20mV

2. The output voltage is noted by varying the input signal frequencies from 20Hz – 20kHz.

3. The voltage gain is calculated by using the formula

   Voltage Gain = 20 log (V_o / V_{in})

4. Mid band gain is noted from the frequency response characteristics

5. Bandwidth is estimated from the frequency response characteristics (Refer model graph)

Result

A FET common source amplifier was constructed and tested. The frequency response characteristic was studied. The voltage gain and bandwidth were estimated.

Parameter	Theoretical Value	Measured Value	Unit
Voltage Gain			
Bandwidth			

Questions

1. What is the difference between FET and BJT?
2. What is the advantage of using FET amplifier?
3. What is the Bandwidth of an amplifier?
4. Explain why the gain is expressed in dB?

Exp. No:
Date:

DESIGN AND TESTING OF RC PHASE SHIFT OSCILLATOR

Aim

To construct RC-phase shift oscillator circuit and to compare the experimental output voltage frequency with the design value of theoretical frequency of the oscillator.

Apparatus Required

Power Supply: (0-12V) DC.
CRO

Components Required

Resistor: 1k, 2k, 10k, 33k-0.5 watts
Capacitor: 0.01μF, 25 μF
Transistor: SL100
probe

Positive Feedback

The block diagram of feedback system is shown in Fig.1. in which the loop gain kA_v is negative.

The overall gain with feedback, $\frac{V_o'}{V_i}$ is shown to be

$$A_{Vf} = \frac{V_o'}{V_i} = \frac{A_V}{1 - kA_V},$$

where A_V is the amplifier gain, $\frac{V_o'}{V_i'}$, and k is the portion of the output voltage fed back to the input. Obviously, if kA_v is negative, the overall gain is reduced. But when kA_v is positive, it provides positive feedback. However the effect of positive feedback

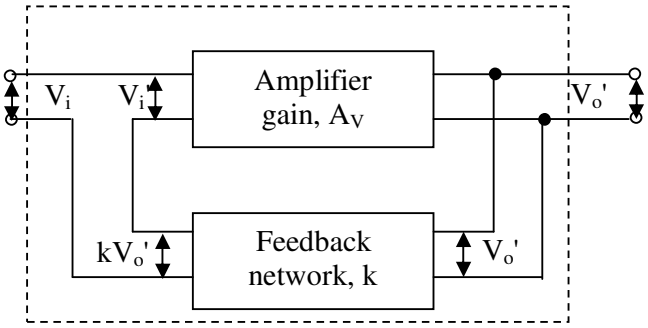


Fig.1. Block Diagram of a Feedback System

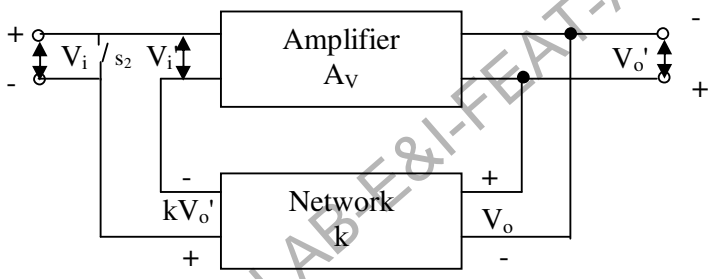


Fig.2. Block Diagram of an Oscillator in which both A_V and K are negative

on the amplifier performance depends on how much feedback is introduced, as shown by the following typical calculations.

Consider $A_v = 40$ and $k = 0.01, 0.02, 0.025$

Case(i) $A_{vf} = \frac{40}{1 - 0.01 \times 40} = \frac{40}{1 - 0.4} = \frac{40}{0.6}$

$= 66.7$

Case(ii) $A_{vf} = \frac{40}{1 - 0.02 \times 40} = \frac{40}{1 - 0.8} = \frac{40}{0.6}$

$= 220$

Case(iii) $A_{vf} = \frac{40}{1 - 0.025 \times 40} = \frac{40}{1 - 1} = \frac{40}{0}$

$= \infty$

This shows that the gain will increase with a larger amount of positive feedback until a critical stage is reached where seemingly the gain is infinite. Assuming that the feedback network is frequency selective network, the infinite gain is achieved for a particular frequency. So the particular frequency is sustained at the output of the amplifier. In other words, the circuit has stopped amplifying and started oscillating. At this stage, the input is removed, and the output will continue. Its frequency depends upon the feedback network or the amplifier, or both.

Requirements for Oscillation

In practice, it is not sufficient just to make $kA_v=1$ in the equation,

$$A_{vf} = \frac{A_v}{1 - kA_v}$$

kA_v is made slightly larger than 1, at which the above equation does not hold good, since the circuit no longer acts as an amplifier.

Since k cannot usually be greater than 1 (if k is an attenuation network), then, $kA_v \geq 1$ means that $A_v \geq 1/k$.

Say that 1.5% of the output of an amplifier is fed back positively to the input. The minimum gain of the amplifier for oscillations to occur is

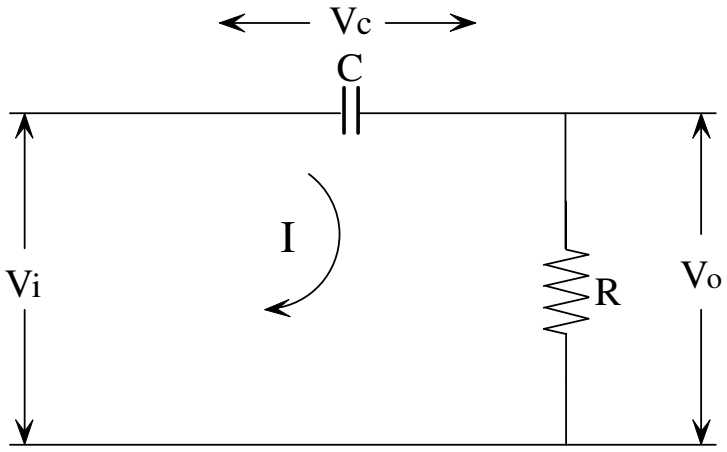


Fig. 3. Single RC Network

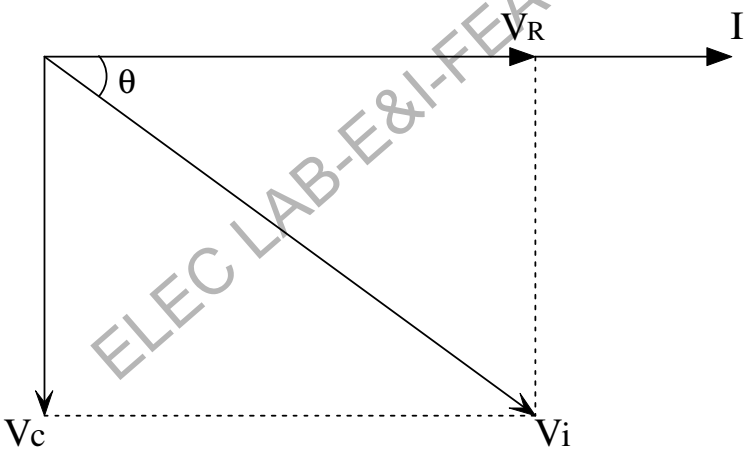


Fig. 4. Phasor Diagram of RC Network

$$A_v \geq \frac{1}{k} = \frac{1}{0.015} = \frac{100}{1.5} = 66.6$$

Actually, if $kA_v > 1$, the gain of the whole system will adjust itself until $kA_v = 1$.

Thus, if $A_v = 100$ and $k = 0.005$ (0.5%), $kA_v = 0.5$, and the circuit will not oscillate. But if the feed back is increased to 2%, (k=0.02) and the system will continue to oscillate, since $kA_v=2$, which meets the requirement for oscillation. For linear oscillations, in which the output is relatively free from distortion, KA_v should be slightly greater than one.

Consider the diagram in Fig.2. in which the amplifier causes a phase shift of 180°between v_i and v_o' (A_v is negative as in a single stage CE amplifier). In order to provide positive feedback, the feedback network must provide a phase shift of another 180° so as to provide a signal that can replace v_i', and not cause more attenuation than $1/A_v$, since kA_v must be equal to or greater than 1. This condition of unity loop gain, ($kA_v=1$), is called the Barkhausen criterion for oscillation and may be met by k and A_v being both positive or both negative. When this criterion is satisfied, switch S-2 can be closed which in turn removes and the output will continue. Its frequency may be different, depending upon the particular circuit components.

If the frequency of oscillation, ($kA_v \geq 1$) is met at only one frequency (due to frequency selective components in the feedback network or amplifier), sinusoidal oscillations will result, and hence a sine wave oscillator. If the frequency is met over a band of frequencies, then the output may be non sinusoidal in wave from, such as a square wave, triangular wave, trapezoidal wave etc.

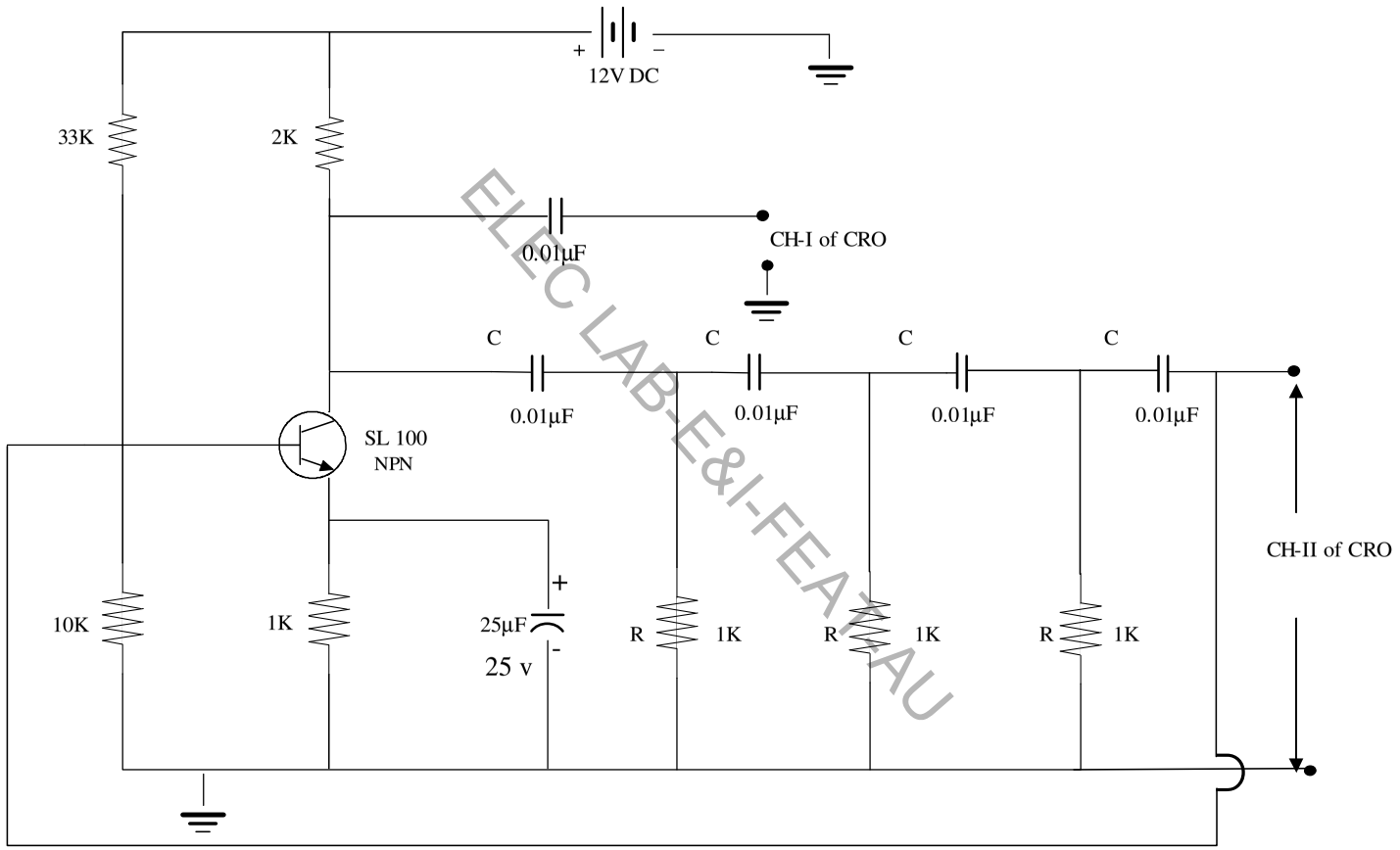


Fig.5. Circuit Diagram of RC Phase Shift Oscillator

Derivation of Frequency Formula

Let us take one RC network as shown in Fig.3.. Let I be the current flowing through the RC circuit. The phasor diagram of the circuit is as shown in fig 2. Taking I as the reference vector, V_o is in-phase with 'I' and V_o is θ^o ahead of V_i and represents a phase shift of θ^o.

To find θ^o

From figure 2, $\tan\theta^o = \frac{Vc}{Vo}$, Where $V_c = I \cdot X_c$ and $V_o = I \cdot R$

Therefore, $\tan\theta^o = \frac{1}{2\Pi fRC}$

Assuming 60^o phase shift from a single RC circuit.

$$\tan 60^o = \frac{1}{2\Pi fRC}$$

$$\sqrt{3} = \frac{1}{2\Pi fRC}$$

Therefore, $f = \frac{1}{2\Pi\sqrt{3}RC}$

If we include the additional current that flows through 'C' for the other sections, then the frequency is given as

$$f = \frac{1}{2\Pi\sqrt{6}RC}$$

$$f = \frac{1}{2\times\Pi\times\sqrt{6}\times R\times C}$$

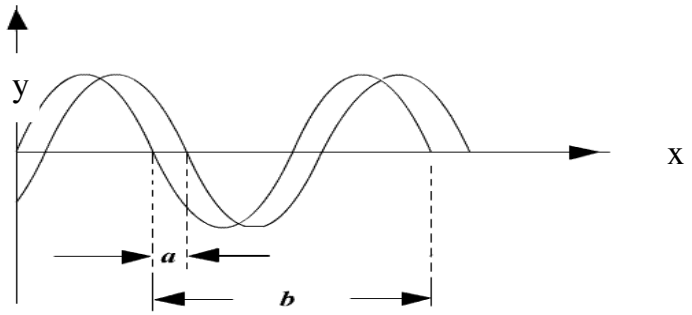


Fig.6. To calculate phase difference from waveform

Specifications Of SL 100 NPN Transistor

Absolute maximum ratings

BV_{CBO} (V) = 60 V, BV_{CER} (V) = 50 V, BV_{EB0} (V) = 6.0 V, Ic (A) = 0.5 A

Surge (A) = 1.0 A, I_{CBO} (A) = 1.0 mA, h_{FE} = 40/300, V_{CE} = 5 V, I_C = 150 mA

Maximum Collector dissipation at Tc = 25 ^{o} is 40W.

Determination of Feedback Circuit Parameters for given frequency

Assume the frequency (f) of oscillator to be produced is 6.5kHz

Given f=6.5kHz=6.5×1000Hz

Take C=0.01μF= 0.01×10^{-6} F

$$6.5\times1000 = \frac{1}{2\times\Pi\times\sqrt{6}\times R\times0.01\times10^{-6}}$$

R≈1000Ω=1k

Precautions

1. Check the polarity of the power supply
2. Identify the transistor terminals properly
3. The DC power supply should not exceed 12Volt.

Procedure

1. Give connections as per the circuit diagram shown in fig 5.
2. Connect the collector of the transistor to the channel-1 of CRO.
3. Switch on the power supply.
4. Trace the waveform and find the frequency of waveform using CRO.
5. Now connect the channel-II of CRO to the output of the 1st RC then to 2nd RC and then to 3rd RC and calculate the respective phase difference of each RC network.
6. Compare the phase difference and frequency of the waveform with theoretical values.

Phase Difference from the Waveform

1. Adjust the CRO settings (Time/Div and Volts/Div knobs). Obtain the waveforms, Shown in fig 6. Trace the waveforms.
2. Now calculate the phase angle (ϕ) as $\phi = 360 * \frac{a}{b}$.

   Where **a** – No. of divisions between collector output and RC network waveforms.

   b- Time period of the wave form.
3. Repeat the procedure to obtain phase shift for other RC networks with collector output.

Result

The given RC phase shift oscillator is tested and the phase shift at each RC network was verified.

Exp. No:
Date:

DESIGN AND TESTING OF COLPITT'S OSCILLATOR

Aim

To construct Colpitt's Oscillator circuit and to compare the experimental output voltage frequency with the design value of theoretical frequency of the oscillator.

Apparatus Required

Power Supply: (0-12V) DC.

CRO

Components Required

SL 100 NPN Transistor

Resistors: 330 Ω, 220 Ω, 3.3kΩ, 100 Ω

Capacitors: 0.08 μF, 10 μF, 100 μF

Inductor: 23 mH, 0.1H

Probe

Principle of Operation

The Colpitt's oscillator is shown in fig.1. The ciruit can be recognized as the two wire connected capacitor C1 and C2 provided by a split starter adjustable capacitor with the rotor grounded. In this way a stable circuit can be built which may be used as a load oscillator on super heterodyne type radio receivers.

Frequency of oscillation is given by

$$f = \frac{1}{2\Pi\sqrt{LC}}$$

Where L=L+M M is mutual inductance which can be ignored

and $C = \frac{C_1 \times C_2}{C_1 + C_2}$

The resultant frequency depends upon the natural frequency of the Quartz, Piezo electric crystals.

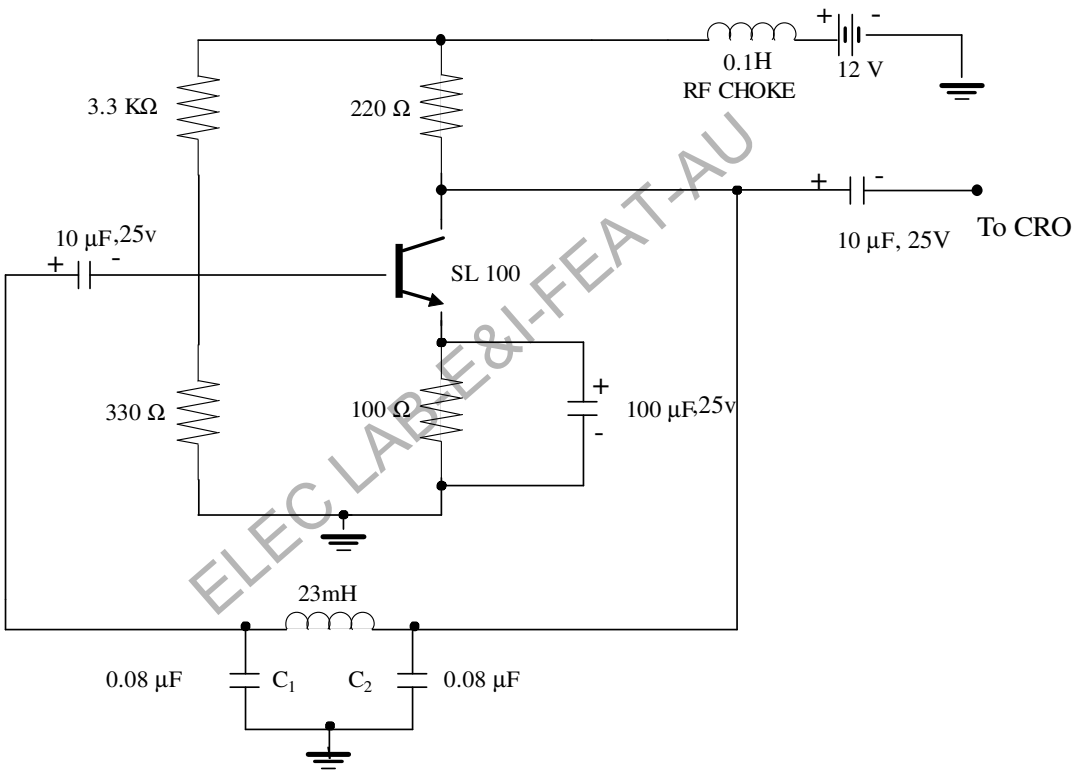


Fig.1. Circuit Diagram of Colpitt's Oscillator

Derivation of Frequency Formula

$X_L = X_C$

$$2\pi fL = \frac{1}{2\Pi fC}$$

$$f = \frac{1}{2\Pi\sqrt{LC}} \qquad \text{Where C} = \frac{C_1 \times C_2}{C_1 + C_2}$$

Specifications Of SL 100 NPN Transistor

Absolute maximum ratings

BV_{CBO} (V) = 60 V, BV_{CER} (V) = 50 V, BV_{EB0} (V) = 6.0 V, Ic (A) = 0.5 A

Surge (A) = 1.0 A, I_{CBO} (A) = 1.0 mA, h_{FE} = 40/300, V_{CE} = 5 V, I_C = 150 mA

Maximum Collector dissipation at Tc = 25 ^{o} is 40W.

Determination of Feedback Circuit Parameters for given frequency

Assume the frequency(f) of oscillation to be produced is 5.3kHz

Given f=5.3KHZ=5.3×1000Hz

Take $C_1 = C_2 = 0.08$ μF

Therefore $C = \frac{C_1 \times C_2}{C_1 + C_2}$

$$C = \frac{0.08\times10^{-6} \times 0.08\times10^{-6}}{0.08\times10^{-6} + 0.08\times10^{-6}}$$

C = 0.04 μF

$$f = \frac{1}{2\Pi\sqrt{LC}}$$

$$5.3\times1000 = \frac{1}{2\times\Pi\sqrt{L\times0.04\times10^{-6}}}$$

$L \approx 2.9\times1O^{-3}H = 2.9mH$

Precautions

1. Check the polarity of the power supply
2. Identify the transistor terminals properly
3. The DC power supply should not exceed 12Volt.

Procedure

1. Give the connections as per the circuit diagram shown in Fig. 1.
2. Connect the output to the y-plates of the CRO
3. Energize the circuit
4. Trace the output waveform and calculate the frequency
5. Compare the theoretical and practical frequencies

Result

The Colpitt's oscillator is constructed,tested and the frequency of oscillation was estimated.

Theoretical Frequency	Measured Frequency	Unit

Exp. No:
Date:

DESIGN AND TESTING OF ASTABLE MULTIVIBRATOR USING BJT

Aim

1.To design an astable multivibrator circuit to generate a square waveform of given frequency.

2.To construct and test the designed astable multivibrator circuit

3.To measure the frequency of the square wave generated and compare it with theoretical value.

Components Required

SK100 PNP transistor - 2 Nos
47 kΩ resistors - 2 Nos
1kΩ resistors - 2 Nos
0.01 μF capacitor - 2 Nos
Regulated Power Supply.

Theory

Astable multivibrator is a device, which generates square waves of its own without any external triggering pulse. There is no stable state and there are two quasi-stable states. In one quasi-stable state, one transistor conducts (ON state) and the other is in non-conducting state (OFF state) for a prescribed time (T_{ON}). After this time, in the second quasi stable state again for a prescribed time (T_{OFF}). The waveform generated by such a circuit is as shown in Fig.1, the second transistor is turned ON while the first transistor is turned OFF.

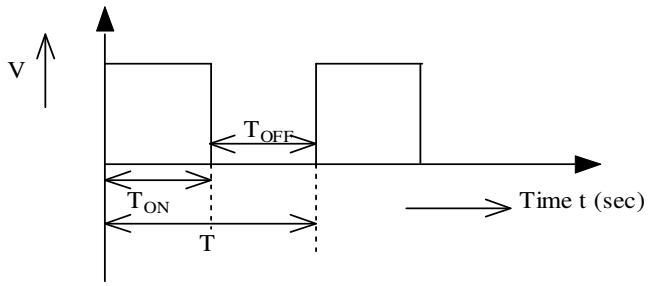


Fig.1. Output Voltage waveform of an Astable Multivibrator

Operation

Practically, no two transistors can have exactly matched characteristics. The current gain h_{FE} of two transistors can never be same. Assuming the transistor T_1 conducts more than transistor T_2, let us analyse the circuit operation. When the power is applied, the current flowing through transistor T_1 is more than the current flowing through transistor T_2. The rising collector current in T_1 drives its collector towards $V_{CE(sat)}$ = -0.2V. This is applied to the base of the transistor T_2 through C_1.This causes a reverse bias on T_2 and thus its collector current starts decreasing the collector voltage of T_2 towards $-V_{CC}$. This is connected to the base of the transistor T_1 through C_2. Thus T_1 is more forward biased. The further increase in collector current of T_1 causes a further decrease of collector current of T_2. This series of action continues until T_1 is driven into saturation and T_2 into cut-off. In this state, point A is at – 0.2V and point B is at $-V_{CC}$. This happens quickly.

When T_1 is ON and T_2 is OFF

When the transistor T_1 is in saturation, the whole V_{CC} drops across R_{C1} i.e., the point. A is at $V_{CE(sat)}$ = - 0.2V. Further, the transistor T_2 is at cut-off i.e., it conducts no current. As there is no voltage drop across $R_{C2,}$ the point B is at - V_{CC}.As point A is at - 0.2V,the capacitor C_1 starts charging through R_{B1} towards $-V_{CC}$ as shown in Fig.2. When the voltage across C_1 becomes more than -0.7V, the transistor T_2 is forward biased and starts conducting.

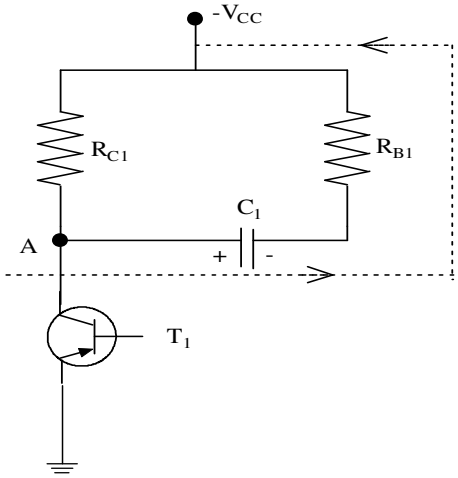


Fig.2.The capacitor Discharge path when T_1 is ON and T_2 is OFF

Quickly, the transistor T_2 is in saturation state while the transistor T_1 becomes cut-off. In this state, the potential of point B decreases from $-V_{CC}$ to -0.2V. The decrease in potential is applied to the base of transistor T_1 through C_2. Consequently T_1 is pulled out of saturation and is soon driven to cut-off. The point A is at a potential $-V_{CC}$. Now T_1 is OFF and T_2 is ON.

When T_1 is OFF and T_2 is ON

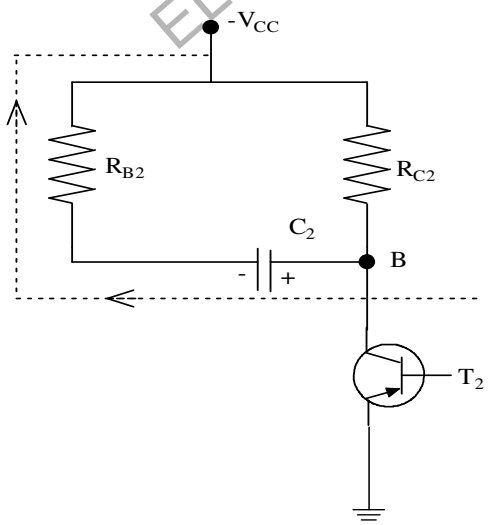


Fig.3. The capacitor discharge path when $T_{1\ is}$ OFF and T_2 is ON

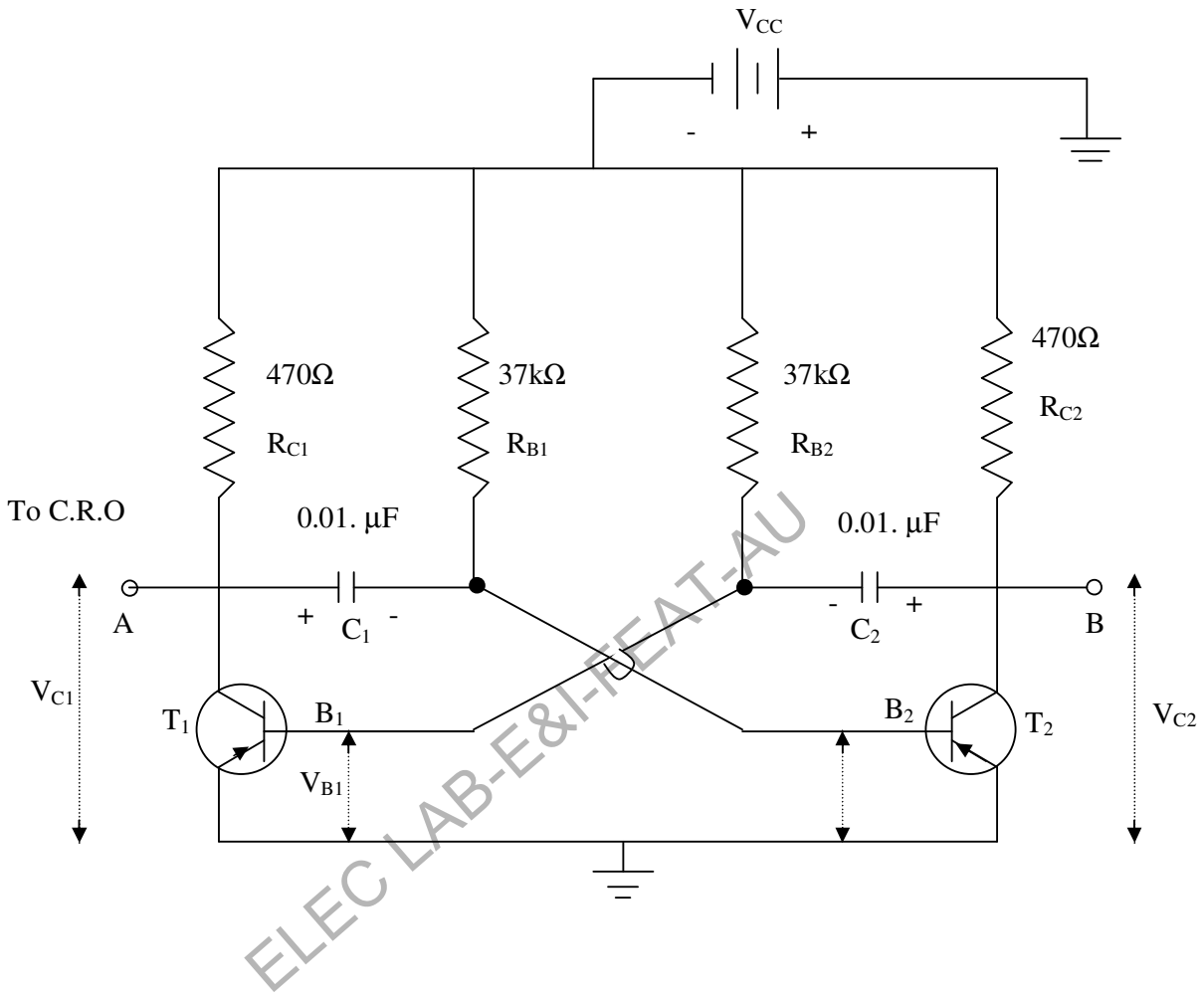


Fig. 5.Circuit diagram of an Astable Multivibrator

As point B is at -0.2V, the capacitor C_2 starts charging through R_{B2} to potential $-V_{CC}$. When the voltage across C_2 is more than -0.7V,the transistor T_1 is forward biased and starts conducting as shown in Fig.3.

The whole cycle is repeated again.

Frequency of oscillations

Let V_C = Capacitor voltage

V_{ini} = Initial capacitor voltage

V_{fin} = Final capacitor voltage

$V_C = V_{ini} + (V_{fin} - V_{ini}) (1-e^{-t/RC})$

$V_C = V_{CC} + (- V_{CC} - V_{CC}) (1-e^{-t/RC})$

[Since $V_{initial} = V_{CC}$ and $V_{final} = -V_{CC}$]

$V_C = V_{CC} - 2V_{CC} + 2V_{CC}\, e^{-t/RC}$

$0 = 2V_{CC}\, e^{-t/RC} - V_{CC}$

$$\frac{1}{2} = e^{-t/RC}$$

$T_{ON} = R_{B1}C \ln (0.5)$

$T_{ON} = 0.69 R_{B1}C_1$

The ON time of transistor T1 or the OFF time of transistor T2 is given by

$T_{ON} = 0.69\, R_{B1}C_1$

Similarly, the OFF time of transistor T1 or ON time of transistor T2 is given by

$T_{OFF} = 0.69\, R_{B2}C_2$

Hence, total time period of square wave

$T = T_{ON} + T_{OFF} = 0.69 (R_{B1}C_1 + R_{B2}C_2)$ ……..(1)

As $R_{B1} = R_{B2} = R$ and $C2 = C_1 = C$, then

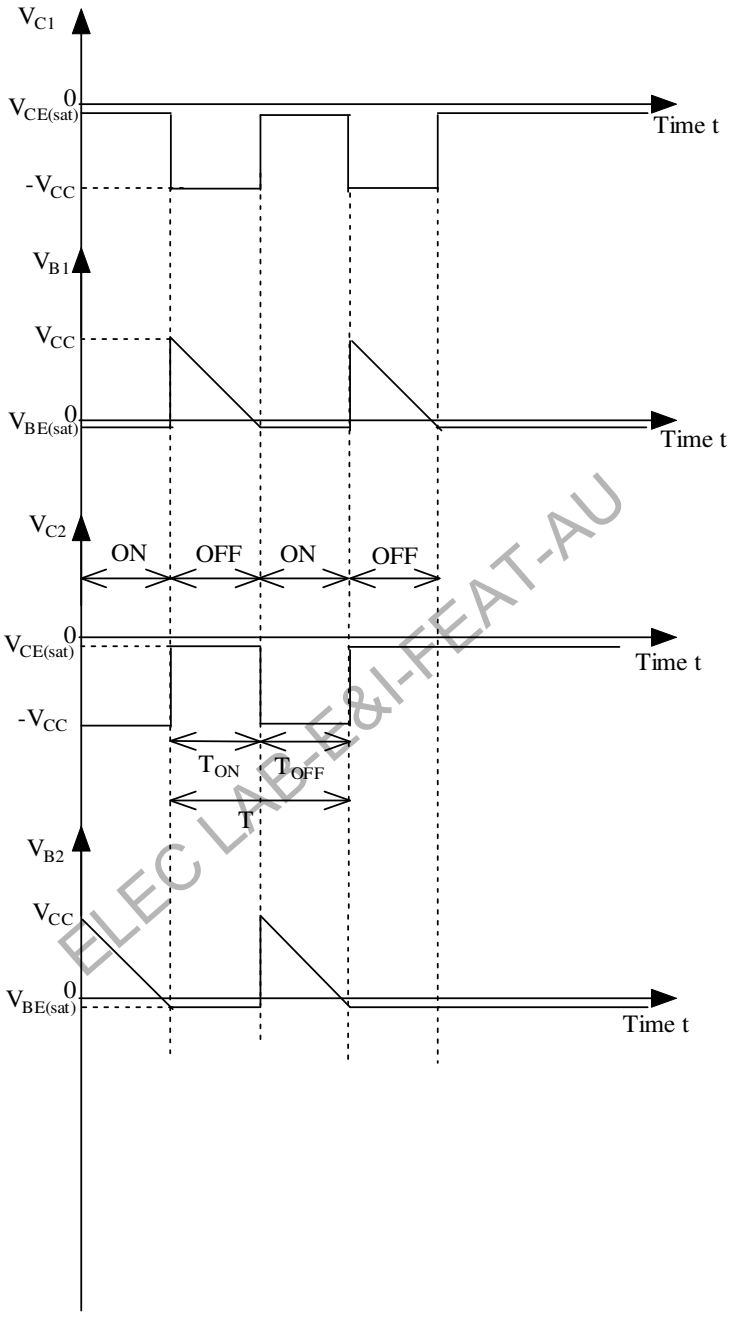


Fig.6. Waveforms at the Collector and Base of transistors

From (1)

$T = 0.69 (R_B C + R_B C) = 1.38 R_B C$

The frequency of square wave

$$f = \frac{1}{1.38 R_B C}$$

Design

Specification

Let V_{CC} =12 V, C = 0.01 μF, f = 2 kHz ,h_{FE} = 80.

(ii).Estimation of R_B:(R_{B1},R_{B2} = R_B)

$$f = \frac{1}{1.38 R_B C} \quad \text{(Choosing C = 0.01 μF)}$$

$$R_B = \frac{1}{1.38 \times 2 \times 10^3 \times 0.01 \times 10^{-6}}$$

R_B = 36.23 kΩ = 37 kΩ

$$I_B = \frac{V_{BB} - V_{BE(sat)}}{R_B}$$

…….. (2)

$$I_B = \frac{12 - 0.7}{37 \times 10^3} = 3.05 \times 10^{-4} A = 0.305 mA$$

[Since VBE = 0.7 V for silicon transistor]

(iii). Estimation of R_C:(R_{C1}, R_{C2} = R_C)

$$I_C = \frac{V_{CC} - V_{CE(sat)}}{R_C} \qquad \text{…… (3)}$$

Also $I_C = I_B h_{FE}$ ……..(4)

(i).Transistor specifications:

SK 100 (PNP) : V_{CBO} = 60 V ; V_{CEO} = 50 V;

I c = 0.5 A max .collector dissipation

Tc = 25°C, h_{FE}(min/max)=40/300

Table.1.

	T_{ON} (Sec)	T_{OFF} (Sec)	Duty cycle $D = \frac{T_{ON}}{T_{ON} + T_{OFF}}$	$F = \frac{1}{T_{ON} + T_{OFF}}$
Theoretical				Hz
Experimental				Hz

$$\%Deviation = \frac{F.Measured - F.Theoretical}{F.Theoretical} \times 100\%$$

From (4)

$$I_C = 3.05\times10^{-4}\times80 = 24.8\text{mA}$$

$$R_C = \frac{12-0.2}{24.8\times10^{-3}} = 475.806\Omega = 470\Omega$$

[Since $V_{CE} = 0.2$ V]

Procedure

1. Make the Connections as shown in Fig.5.
2. Switch on the supply and observe the waveforms at the base ad collector of the two transistors.
3. Measure the T_{ON} and T_{OFF} times from the observed waveforms.
4. Calculate the frequency and compare it with theoretical values.

Result

An Astable multivibrator was designed and tested for frequency of 2kHz. The theoretical and experimental frequencies were verified and values are tabulated in Table.1.The percentage of deviation in the frequency from design value is = ……..

Exercise

1.What is multivibrator? Is it the same as flip-flop?

2.What are the types of multivibrator?

3.What is the other name of astable multivibrator?

4.Can you construct multivibrator using IC? If so, what IC you will choose /

5. How will you vary the frequency of the square wave generated by astable Multivibrator?

6. What is Schmitt trigger?

7.What are the applications of multivibrator?

Exp. No:
Date:

DESIGN AND PERFORMANCE ANALYSIS OF MONOSTABLE MULTIVIBRATOR

Aim

To design a monostable multivibrator for a given ON-time and to test the monostable multivibrator by constructing it in the laboratory.

Components Required

SL100 Transistor		-	2Nos.
Resistor	1kΩ	-	2Nos.
Resistor	20kΩ,7kΩ,8kΩ	-	1No.
Capacitor		-	0.01μF, 100pF

Theory

A monostable or one-shot multivibrator has only one stable state.i.e.one transistor is conducting and the other in non-conducting. The circuit remains indefinitely in this state. When an external triggering pulse is applied, the multivibrator changes from stable state to a quasi-stable state where in it stays for a predetermined time (T_{ON}).

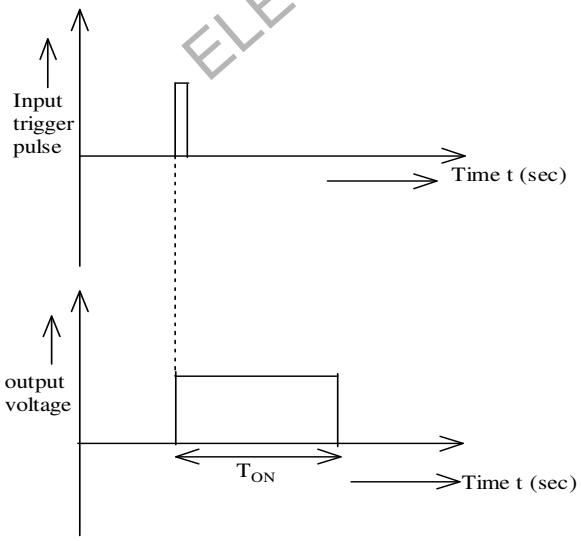


Fig1.Trigger signal and output voltage waveform of monostable multivibrator

After this predetermined time, the multivibrator returns to its original stable state automatically and remains there until another triggering pulse is applied, this is explained in Fig.1.

Operation

Stable state: Transistor T_1 OFF and T_2 ON:

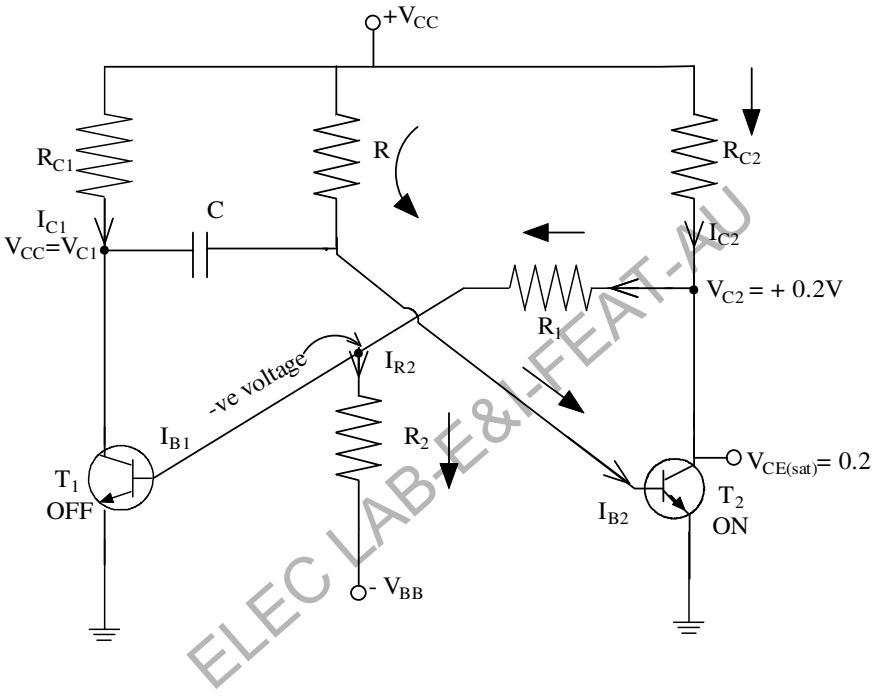


Fig.2 Operation of monostable multivibrator at stable state.

In the stable state, transistor T_1 is OFF and T_2 is ON. This is explained by Fig.2. The voltage source V_{BB} asserts a negative voltage at the base of T_1. This drives the transistor T_1 into cut-off. The transistor T_2 goes into saturation because of the positive voltage applied from V_{CC} to its base through R. Since T1 is OFF, no current flows through RC1 and the collector voltage $V_{C1} = V_{CC}$. Transistor T_2 is in saturation and its collector is at 0.2 V. The base voltage V_{B1} is provided by the potential divider formed by R_1 and R_2.

$$V_{B1} = \frac{R_1}{R_1 + R_2} \times V_{BB}$$

Quasi-Stable State

Assume that a positive pulse is applied at the base of transistor T_1. A capacitor couples this pulse to the base of transistor T_1 and makes T_1 conducting. T_1 quickly goes into saturation pulling its collector voltage down to 0.2 V immediately. This sharpe change in V_{C1} from V_{CC} to 0.2V is coupled through C to the base of transistor T_2 thus driving it into cut-off. Therefore the collector voltage of T_2 goes to V_{CC}. Now the potential divider formed by R_1 and R_2 helps to establish a positive potential holding T_1 in saturation as shown in Fig.3.

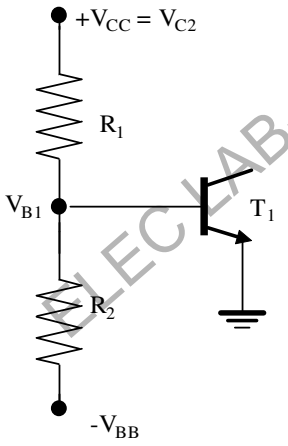


Fig.3.Base biasing when T_1 is ON and T_2 is OFF.

$$V_{B1} = (V_{CC} + V_{BB}) \times \frac{R_2}{R_1 + R_2}$$

Thus the monostable multivibrator has been turned on by a trigger pulse.

Turn –on time

T_1 will stay in this quasi -stable state only for a predetermined time. The capacitor C now begins to discharge through T_1 to ground via R with the polarity as shown in Fig.4. When this voltage goes above 0.7 T_2 goes on again thus making the multivibrator to switch back to the stable state.

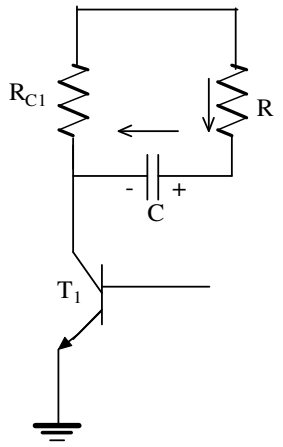


Fig.4.Capacitance charge path when T_1 is ON and T_2 is OFF

Design

Let the supply voltage Vcc = 6V,V_{BB} =1.5V,assume h_{FE} min = 20, Ic(sat) =6 mA T_{ON}= 50msec.

<u>At stable state T_2 is ON and T_1 is OFF:</u>

<u>(i).Estimation of R_{C1} ,R_{C2}:</u>

$$R_{C1} = R_{C2} = \frac{V_{CC} - V_{CE(sat)}}{I_{C(sat)}} = \frac{6 - 0.3}{6 \times 10^{-3}} = 950\Omega = 1k\Omega$$

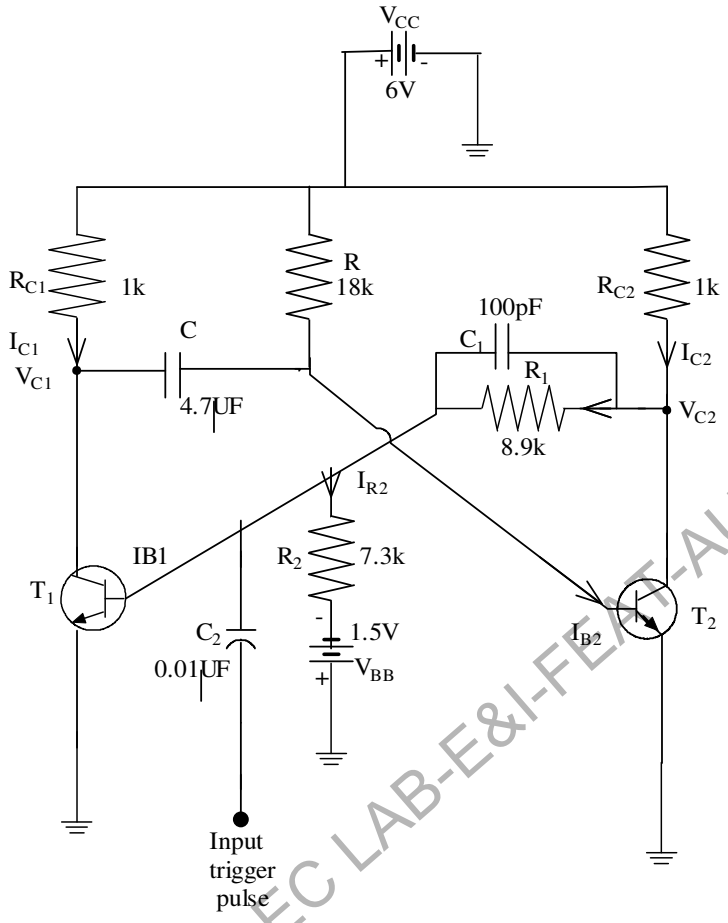


Fig.7.Circuit diagram of monostable multivibrator

$$I_{B2(sat)} = \frac{I_{C(sat)}}{h_{FE(min)}} = \frac{6-0.3}{20} = 0.3mA$$

Also $I_{B1(sat)} = 0.3mA$

(ii).Estimation of R:

$$R = \frac{V_{CC} - V_{BE(sat)}}{I_{B2(sat)}} = \frac{6-0.7}{0.3\times10^{-3}} = 17.67k\Omega = 18k\Omega$$

[$V_{BE\ (Sat)}$ =0.7 for silicon transistor]

<u>At quasi- stable state T_1 is ON and T_2 is OFF:</u>

V_C = Capacitor voltage

V_{ini} = Initial capacitor voltage

V_{fin} = Final capacitor voltage

$V_C = V_{ini} + (V_{fin} - V_{ini}) (1-e^{-t/RC})$

$V_C = V_{CC} + (-V_{CC} - V_{CC}) (1-e^{-t/RC})$

$V_C = V_{CC} - 2V_{CC} + 2V_C$

$$0 = 2V_{CC}\ e^{-t/RC} - V_{CC}$$

$$\frac{1}{2} = e^{-t/RC}$$

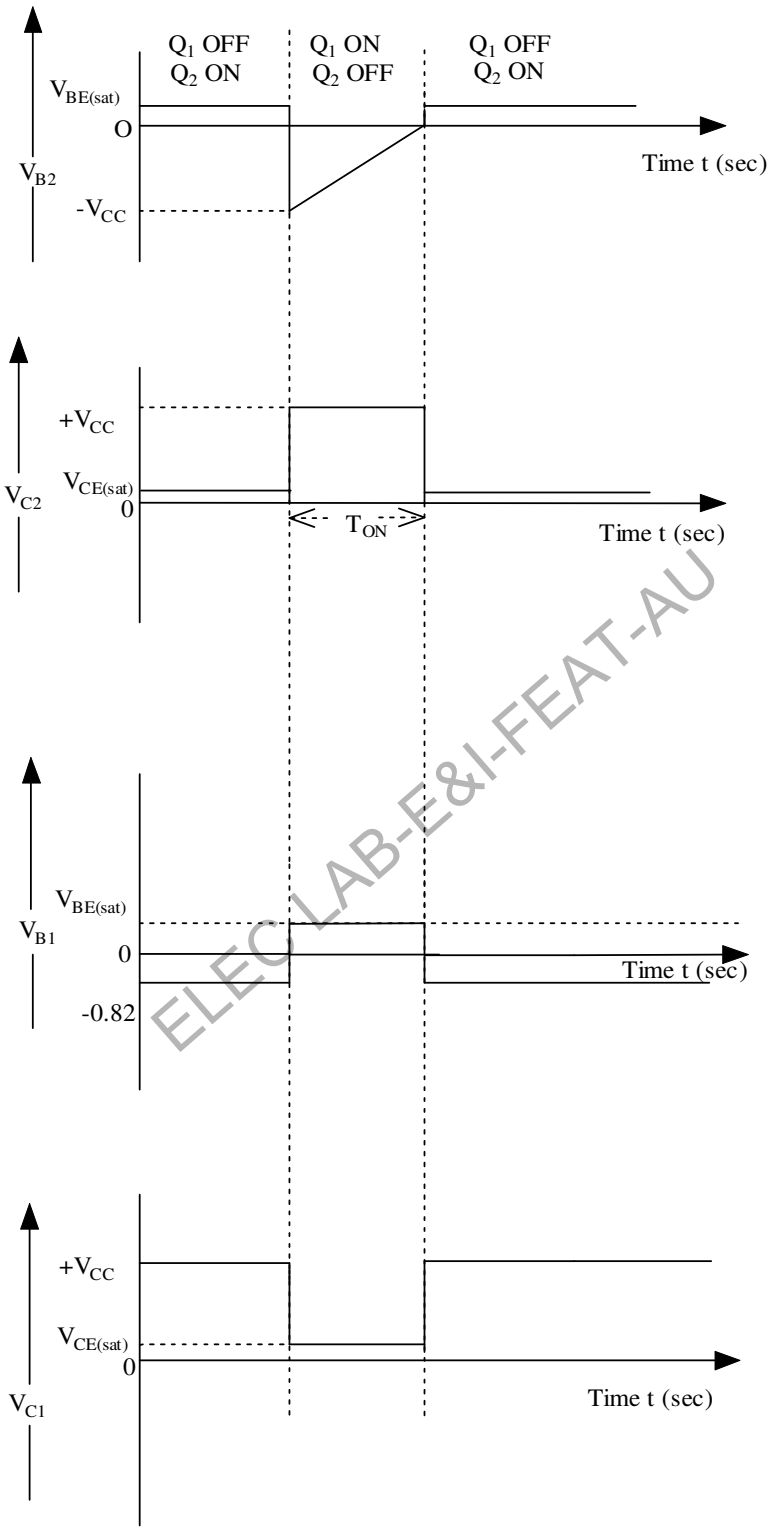


Fig.8. Collector and Base Waveforms

$T_{ON} = RC \ln (0.5)$

$T_{ON} = 0.69RC$ ---------- (1)

From (1)

$$C = \frac{T_{ON}}{0.693R} = \frac{50\times10^{-3}}{0.693\times18\times10^{3}} = 4.7\ \mu F$$

Assume $I_{B1\,(sat)} = I_{B2}$

When T1 is in conduction

$$I_{R1} = I_{B1(sat)} + I_{R2} = 0.3mA+0.3mA = 0.6mA$$

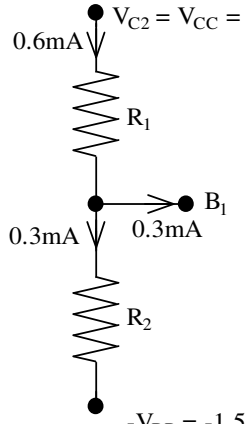


Fig.5.Biasing for T_1 in quasi- stable state

$$V_{B1} = 0.7V$$

(iii). Estimation of R_1 & R_2:

$$I_{R2} \times R_2 = V_{BE(sat)} - (-V_{BB})$$ ---------- (2)

$$0.3mA \times R_2 = 0.7 - (-1.5) = 2.2V$$

$$R_2 = \frac{2.2}{0.3mA} = 7.3k\Omega$$

$$I_{R1} \times R_1 = V_{CC} - V_{BE(sat)} \quad \text{---------- (3)}$$

From (3) and Fig.5.

$$R_1 \times 0.6\text{mA} = 6 - 0.7\text{V}$$

$$R_1 = \frac{5.3\text{V}}{0.6\text{mA}}$$

$$= \frac{5.3}{0.6}\text{k}\Omega = 8.9\text{k}\Omega$$

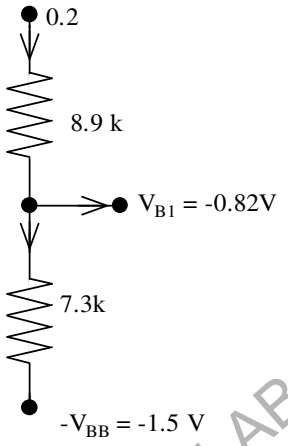


Fig.6.Base biasing condition for T_1 at stable state (T_1 OFF)

$V_{B1} = \frac{8.9}{16.2} \times 1.5 = -0.82\text{V}$ (This negative voltage can help the transistor T_1 OFF. Therefore our design is fine. The speed up capacitor C_1 is chosen such that $R_1C_1 = 1\ \mu\text{F}$ and hence,

$$C_1 = \frac{10^{-6}}{8.9 \times 10^3} = 112.4\text{pF} = 100\ \text{pF}$$

Procedure

1. Make connections as per the circuit diagram shown in fig.1.
2. Switch on the power supply and observe the waveforms at the base and collector of the two transistors at stable state.

3. Now apply a pulse at the base of T_1 and observe waveform.
4. Note down T_{ON} .
5. Compare it with theoretical T_{ON}.

Result

A monostable multivibrator was designed and tested.

	Theoretical T_{ON} (sec)	Measured T_{ON} (sec)
Theoretical		
Experimental		

$$\%Deviation = \frac{T_{ON}.Measured - T_{ON}.Theoretical}{T_{ON}.Theoretical} \times 100\%$$

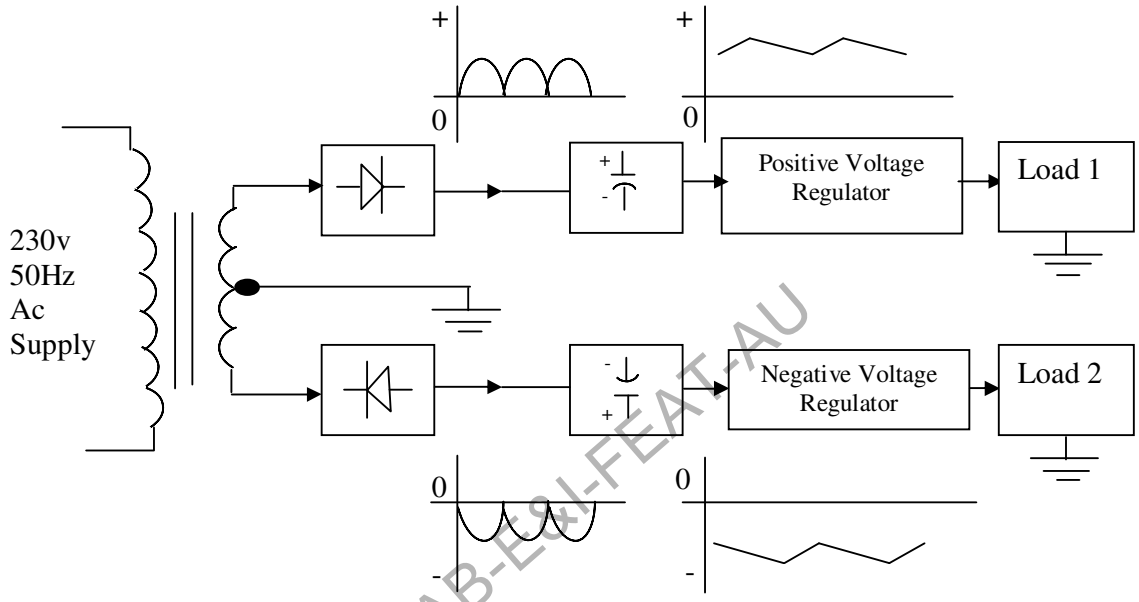


Fig.1. Block Diagram of Regulated Dual D.C. Power Supply

Exp. No:
Date:

DESIGN AND TESTING OF REGULATED DUAL DC POWER SUPPLY AND STUDY OF IT'S LOAD REGULATION CHARACTERISTICS

Aim

To construct a Dual DC Power Supply and to study its load regulation characteristics.

Components Required

N-P-N Transistor	SL100	1No.
	BC147	1No.
P-N-P Transitor	SK100	1 No.
	BC158	1No.
1N 4007 Diode		4 Nos.
Resistor	560, ½ W	2Nos.
	330, ½ W	2Nos.
	100, ½ W	2Nos.
Capacitor	1000 µF,25V	2Nos.

Formula

$$\% \text{ Load Regualtion} = \frac{(V_{\text{no load}} - V_{\text{load}})}{(V_{\text{no load}})} \times 100$$

Precautions

(1) SPST switches are kept open at the time of starting to find the no load output voltage.

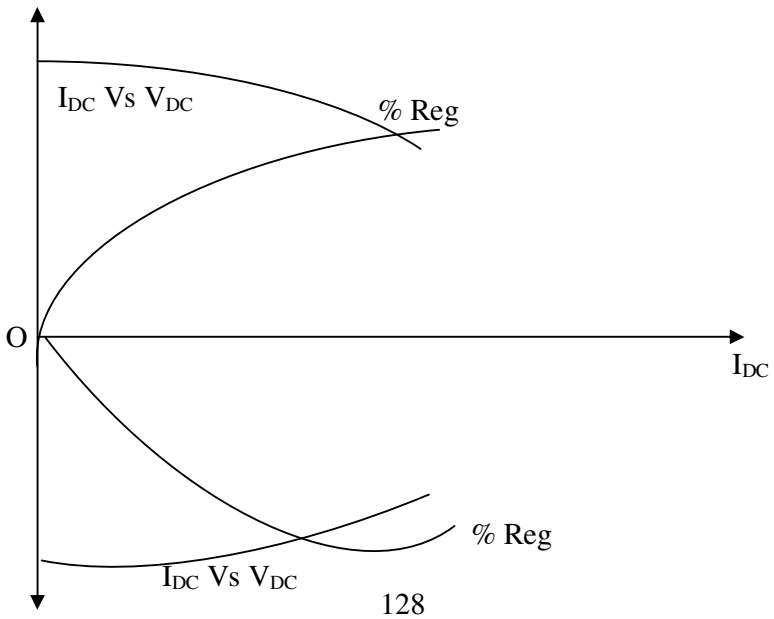
(2) The rheostat (resistive load) should be kept at maximum resistance position.

(3) Do not load both upper and lower part simultaneously.

Tabular Column

V_{noload} = ____V

Positive Voltage Source			Negative Voltage Source		
I_{DC}	V_{DC}	% Regulation	I_{DC}	V_{DC}	% Regulation



Model Graph

Theory

In an unregulated power supply,the output voltage changes whenever the input voltage or load changes. An ideal regulated supply is an electronic circuit desgined to provide a predetermined d.c.voltage V_0 which is independent of the load current and variations in the input voltage. A voltage regulater is an electronic circuit that provides a stable d.c.voltage indepented of the load current, temperature and a.c. line voltage variations.

Load Regulation

$$\% \text{ Regualtion} = \frac{(V_{\text{no load}} - V_{\text{load}})}{(V_{\text{no load}})} \times 100$$

Where $V_{\text{no load}}$ is the output voltag at zero load crrent and $V_{\text{full load}}$ is the output voltage at rated load current. This is usually denoted in percentage.

Procedure

1. The connections are given as per the circuit diagram shown in Fig. 1
2. Energise the primary of the transformer by closing DPST switch.
3. Note down the no load DC output voltage for $I_L = 0$
4. Close the $SPST_1$ switch for positive DC output voltage
5. Vary the load rheostat to set the load current
6. Note down the corresponding DC output voltage
7. Repeat the procedure for ¼, ½, ¾, full load currents and find the corresponding DC output voltage.
8. Fill it in the tabular column
9. Open $SPST_1$ switch
10. Find the % regulation as per formula given.
11. Draw the graph I_{DC} Versus V_{DC} and I_{DC} Versus % Regulation
12. Close the $SPST_2$ switch for negative DC output voltage.
13. Repeat the procedure from step 5 to step 8.
14. Open $SPST_2$ switch
15. Repeat the procedure from step 10 to step 11.

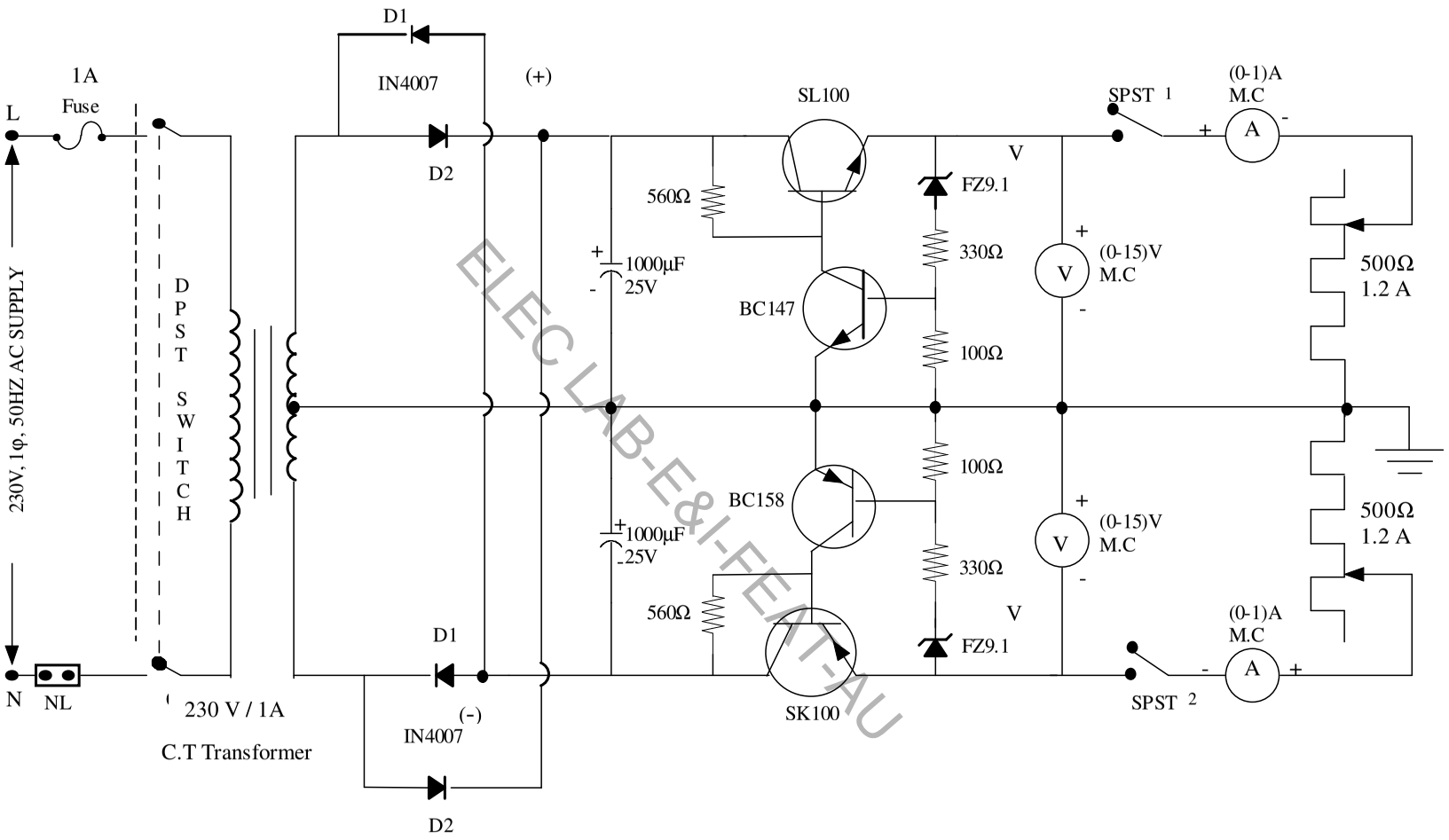
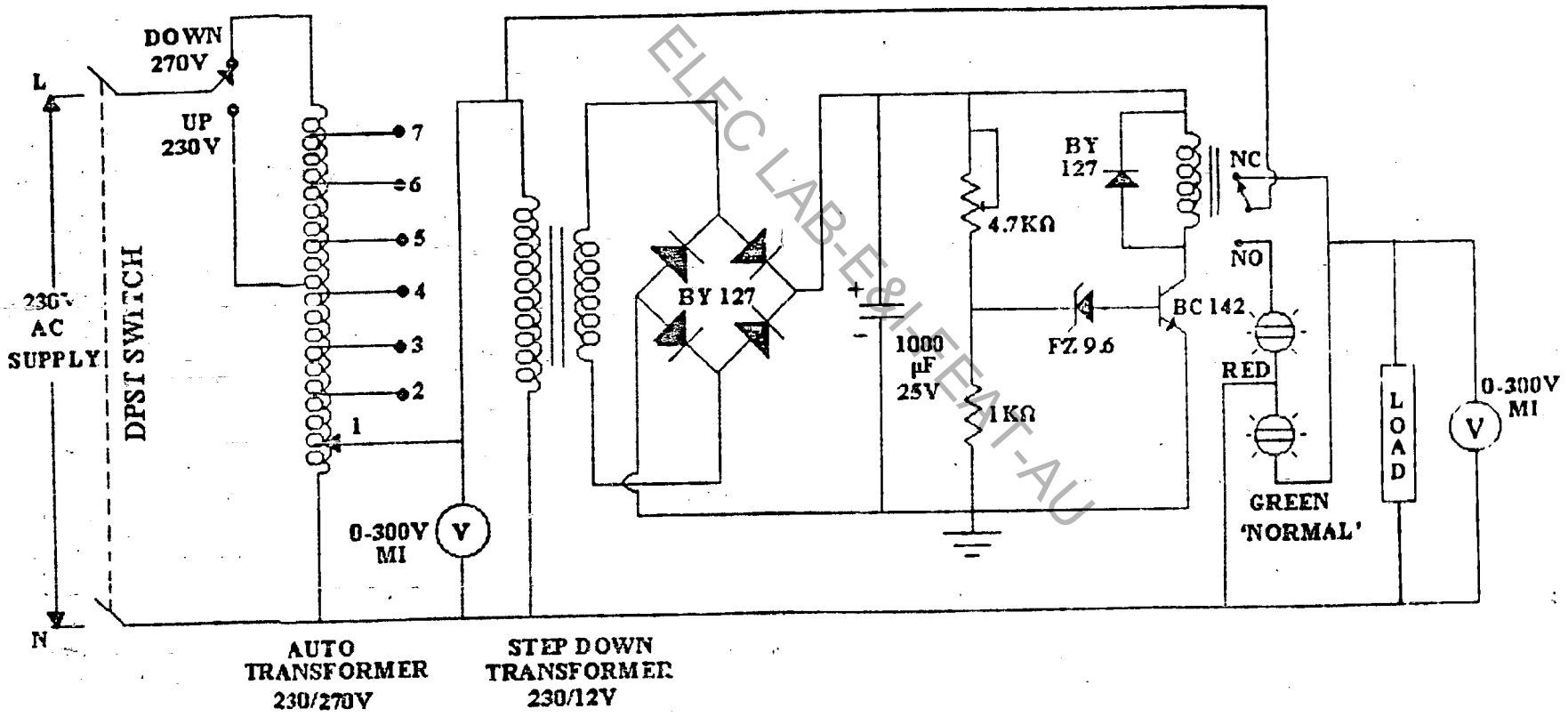


Fig. 2. Circuit Diagram of Dual Regulated D.C. Power Supply

Result

The regulated dual DC power supply was constructed and tested.

FIG.1. CIRCUIT DIAGRAM for AC MANUAL VOLTAGE STABILIZER



Exp No:
Date:

DESIGN OF AUTO CUT-OFF CIRCUIT FOR AC VOLTAGE STABILIZER

Aim

To design and construct an AC voltage stabilizer with auto cut off at 230 volts and to verify its operation.

Components Required

Auto transformer, single pole 8 way switch, 230/12 volts transformer. Diode (1N4001), capacitor (1000μf/25volts) resistors (4.7 kΩ, preset 1 kΩ) relay (6 volts/40 Ω), transistor (BC 147), Zener diode (FZ 9.1 V), red and green lamps, Voltmeter (0-300V MI)

Theory

Need For Voltage Stabilizer

Voltage fluctuations are present everywhere and unless some sort of remedial measures are taken, serious damage to expensive equipment could result. Most of the electrical appliances are designed to operate satisfactorily at 230 volts ac supply. A variation of supply voltage of +/- 10% will not harm most of them. But variation larger than these can cause problem varying from unsatisfactory performance to a total failure of the equipment. For example, a refrigerator (compressor) will not function properly if the supply voltage drops below 190 volts. Similarly a 100 watts tungsten filament bulb in the home would glow as 60 watts when there is a drop in supply voltage. Also we can observe that the fan is revolving with lesser speed due to supply voltage drop. Hence a voltage stabilizer can be used to counteract the problem of voltage fluctuations. A manual voltage stabilizer with higher voltage cut off (240 volts) can be constructed as explained in this experiment.

Tabulation

Cut Off Voltage = 230 Volts

Sl.No.	Measured I/P voltage	Status of green lamp	Status of red lamp	Measured O/P voltage
1.	150			
2.	160			
3.	170			
4.	180			
5.	190			
6.	200			
7.	210			
8.	220			
9.	230			
10.	240			

Position Up

Sl.No.	O/P voltage

Position Down

Sl.No.	O/P voltage

Working of Auto Cut-Off Circuit

In this circuit 230 volts ac supply is stepped down to 12 volts ac by 230/12 volts transformer and rectified by a diode bridge rectifier and then filtered by a capacitor. Under normal operation the dc voltage available is 12 volts. The Zener diode which is used as a comparator has a breakdown voltage of 9.1 volts and the transistor has a voltage drop of 0.7 volts at $V_{B\,E.}$

The voltage at point A should to be minimum 9.8 volts to make the transistor on. During normal operation, transistor is less forward biased and hence acts as an open circuit. Hence the base current of the transistor is Zero ($I_B = 0$) and the current which will energize the relay coil is not enough since transistor is off. Therefore the relay is in normal closed position and hence the green lamp glows indicating the normal operation. Now the voltmeter connected at the output reads the output voltage. But when the supply voltage increases, the dc voltage at point A exceeds 9.8 volts making the Zener to breakdown and drives the base of the transistor which causes collector current to flow making $V_{CE} = 0$ and $I_C = I(sat)$. This collector current energizes the relay coil and hence, relay switches its state from normally closed to normally open. Hence, green lamp doesn't get ac supply where as red lamp gets ac supply and glows there by indicating the auto cutoff operation. Under this condition the voltmeter connected at the output indicates 0 volts. This auto cut off circuit operates only when there are supply voltage fluctuations.

Procedure

1. Connect 230 volts ac supply to the sockets provided.
2. The voltmeter connected at the input side reads the input voltage.
3. If the input voltage is below 230 volts, then throw the single pole 2 way switch to the "UP" position and use the single pole 8 way switch to increase the input voltage. While doing so, observe the auto cut off at 240 volts input shown by the glow of red lamp indicator and the voltmeter at the input side reads the voltage at

cut off. Now the voltmeter at the output side reads zero volts.

4. If the input side voltmeter shows input voltage above 230 volts, (since the single pole 2 way switch is already in "DOWN" position) then use the single pole 8 way switch to decrease the input voltage and observe the auto cutoff at 240 volts indicated by the glow of red lamp and note down the reading of voltmeter at the input side as 240 volts and the voltmeter at the output reads zero volts.
5. Under normal operation, when the input is 230 volts, the green lamp glows and the voltmeter reads the output voltage.

Result

Auto cut off circuit for AC voltage stabilizer was constructed for a cut-off voltage of 230V and its operation was verified.

Exercise

1. What is a stabilizer?
2. What are the types of stabilizer?
3. Is a stabilizer differ from voltage regulator?
4. What is the function of Zener diode auto cutoff circuit?
5. Why should a diode is connected across the relay coil?